

Model Name: P35-S3G

Revision 1.0

SHEET TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	P4 LGA775 A
05	P4 LGA775 B,D
06	P4 LGA775 C
07	P4 LGA775 E,F,G,H
08	GMCH-BEARLAKE HOST
09	GMCH-BEARLAKE DDRII
10	GMCH-BEARLAKE PCI E, DMI
11	GMCH-BEARLAKE VGA
12	GMCH-BEARLAKE GND
13	GMCH-BEARLAKE PWR
14	PCI EXPRESS*16 SLOT
15	DDRII CHANNEL A 1,2
16	DDRII CHANNEL B 1,2
17	DDRII TERMINATION
18	ICH9 PCI, USB, DMI, LAN
19	ICH9 GPIO, CTRL
20	ICH9 SATA, FAN PWM
21	ICH9 VCC, GND
22	CLOCK GEN CK505
23	PCI EXPRESS*1 ,PCI SLOT 1,2
24	FDD/F USB
25	ITE8718GB
26	COM,LPT
27	BIOS,CI,HWM,KB/MS

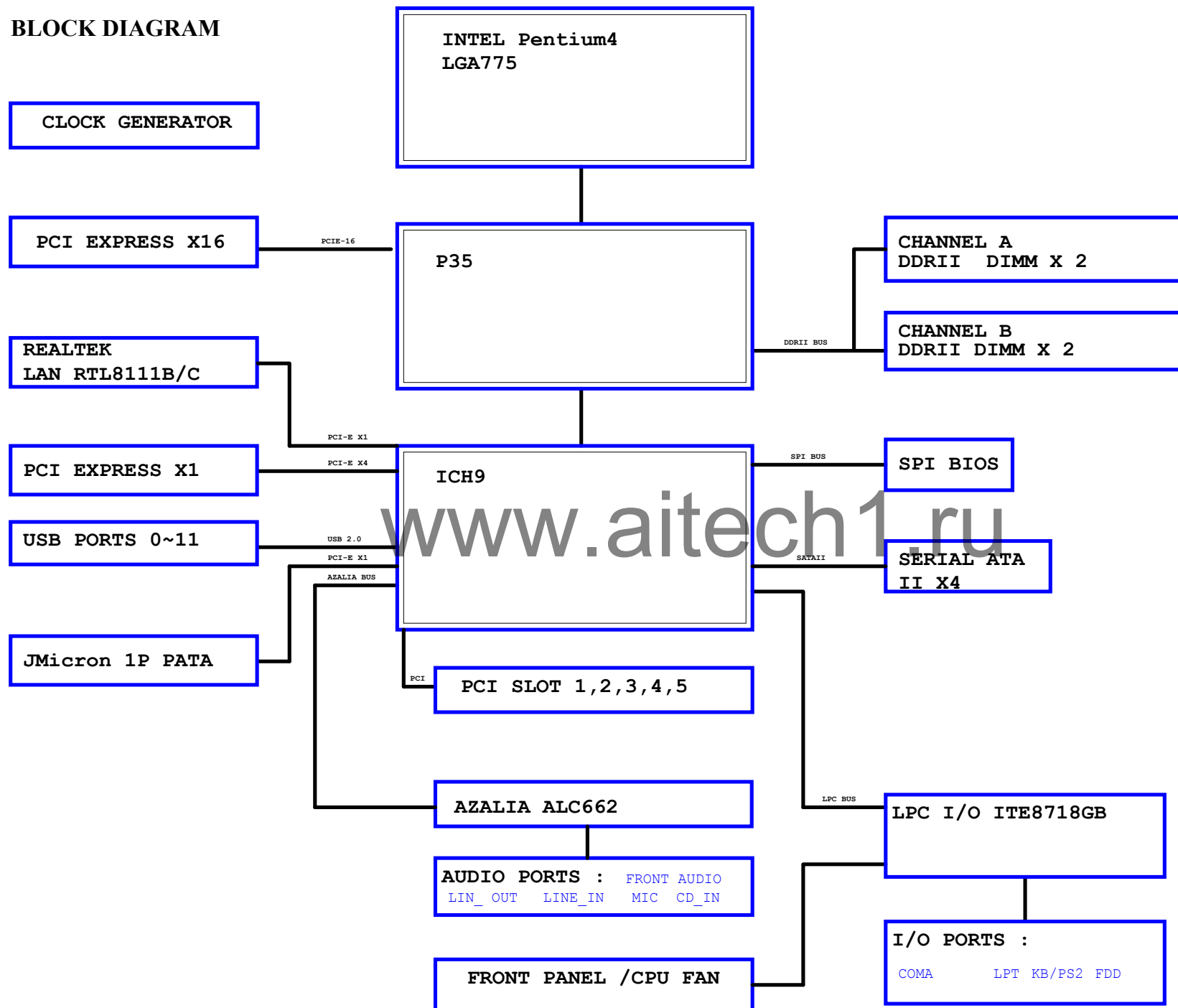
SHEET TITLE

28	AZALIA ALC662
29	AUDIO JACK
30	DISCRETE POWER
31	VCORE PWM ISL6312-3 PHASE
32	ATX POWER
33	FRONT PANEL,FUSB,FDD
34	JMicron 1P PATA-JMB368
35	LAN REALTEK RTL8111B/C
36	PCI SLOT 3,4,5

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Gigabyte Technology		
Title		
Cover Sheet		
Size	Document Number	Rev
Custom	P35-S3G	1.0
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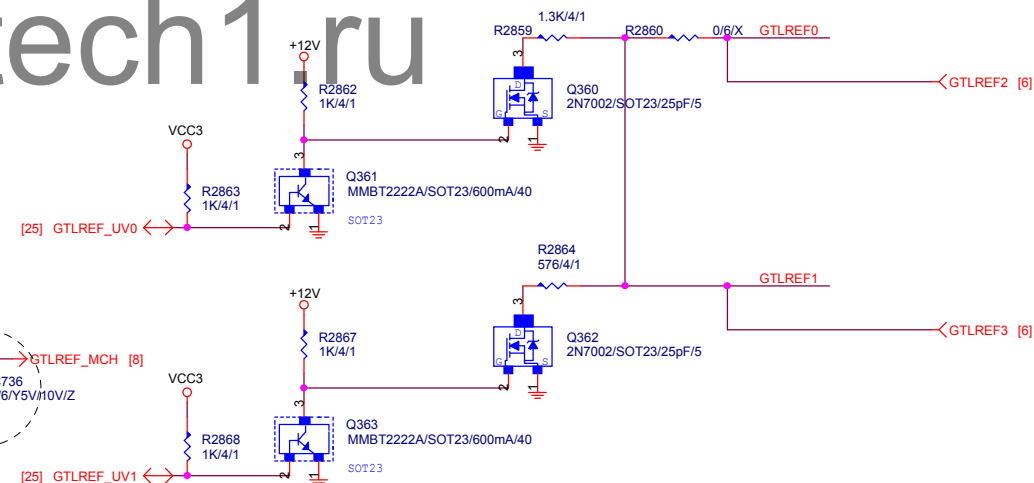
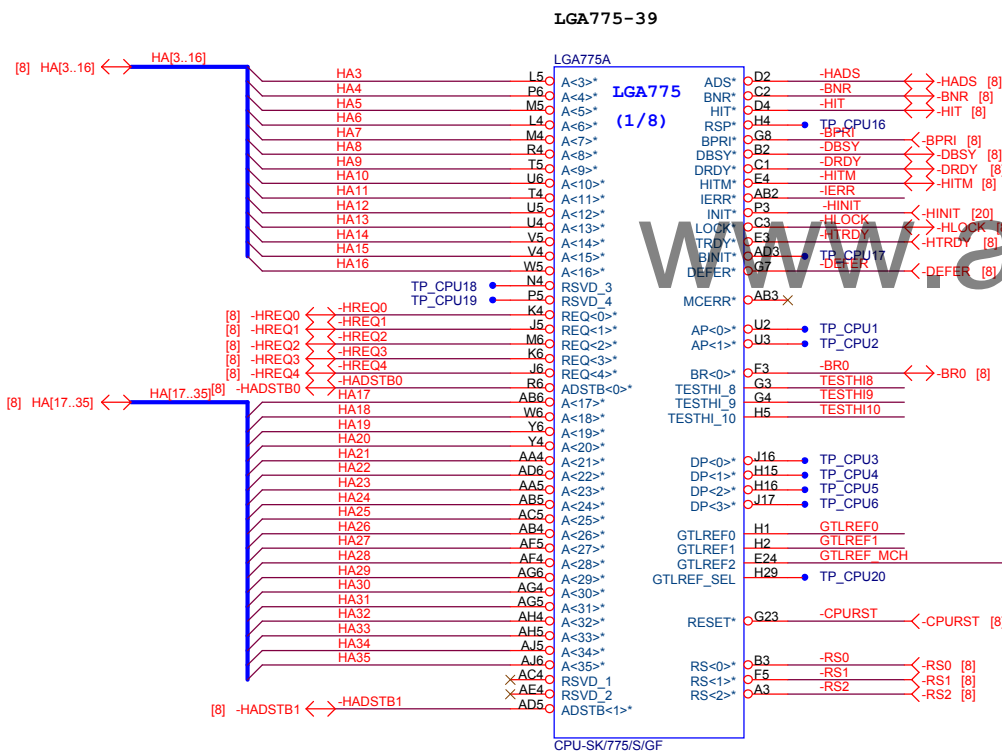
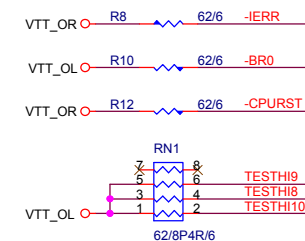
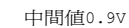
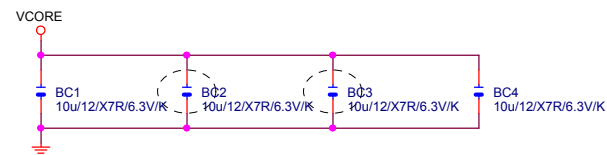
BLOCK DIAGRAM



Version: 1.0

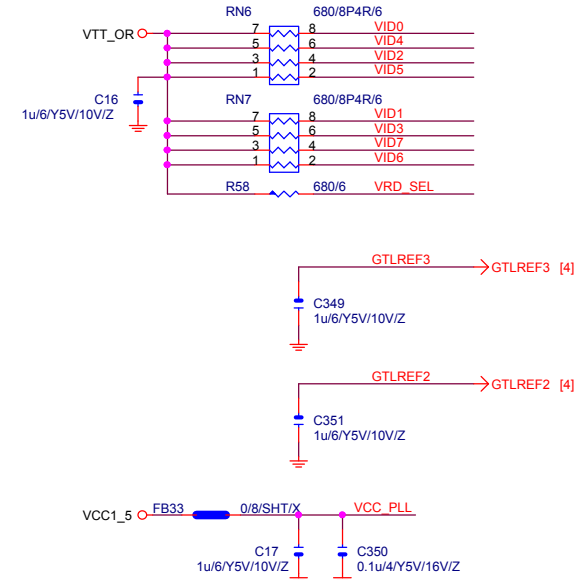
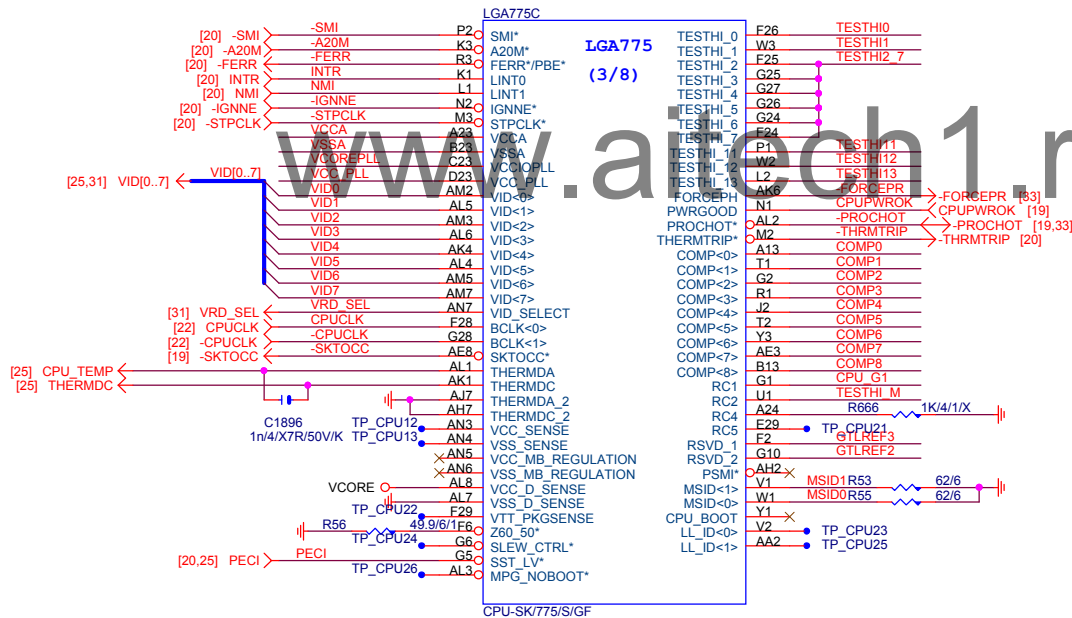
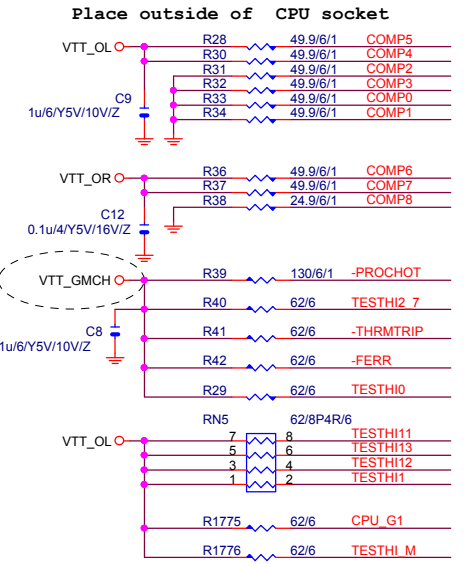
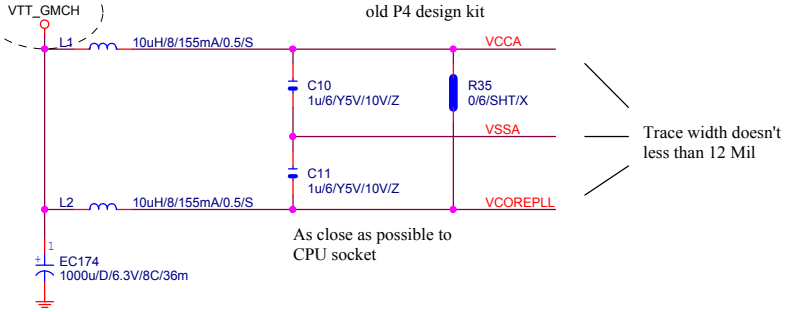
2007/11/15

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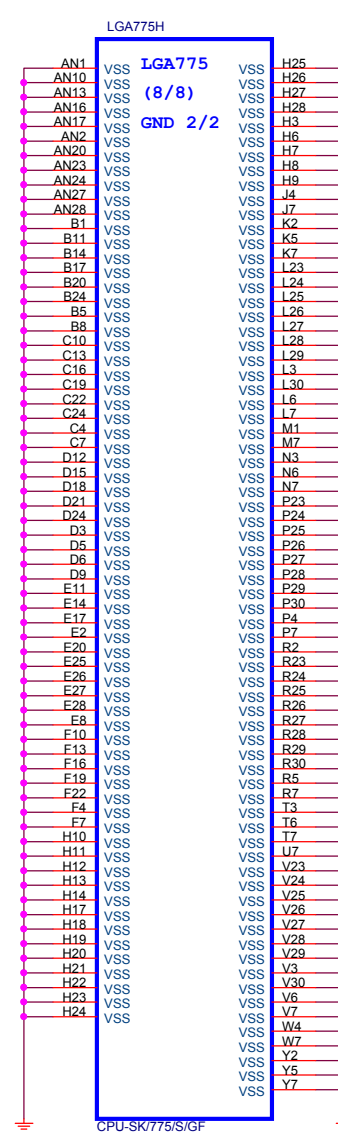
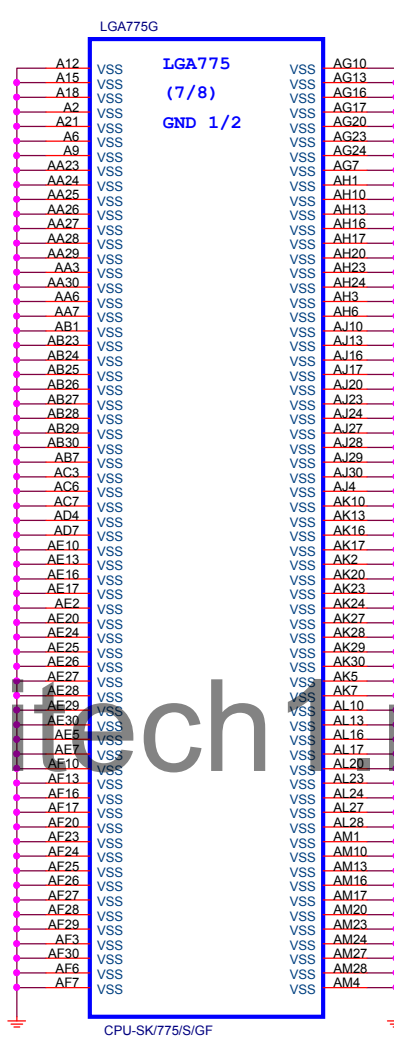
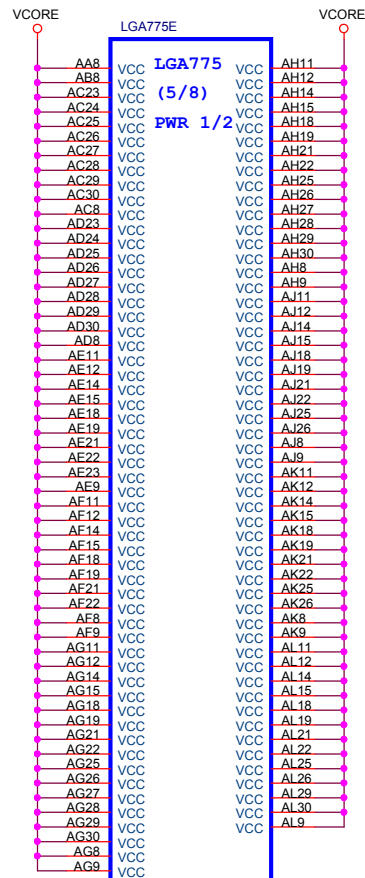
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Size B	<p>Document Number</p> <p align="center">P35-S3G</p>			Rev 1.0
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Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit

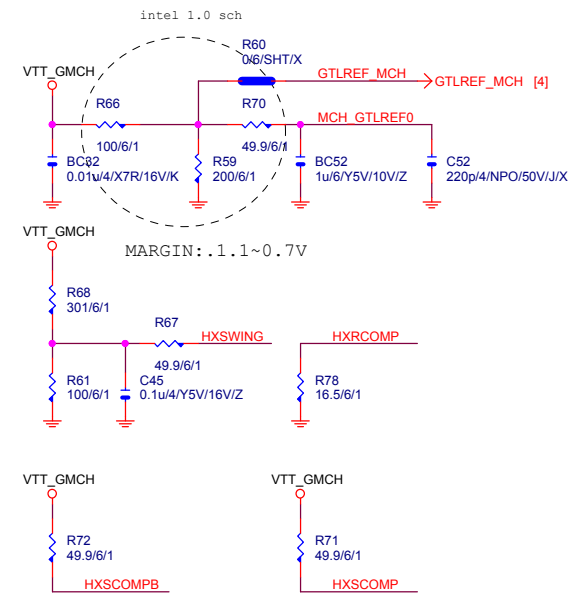
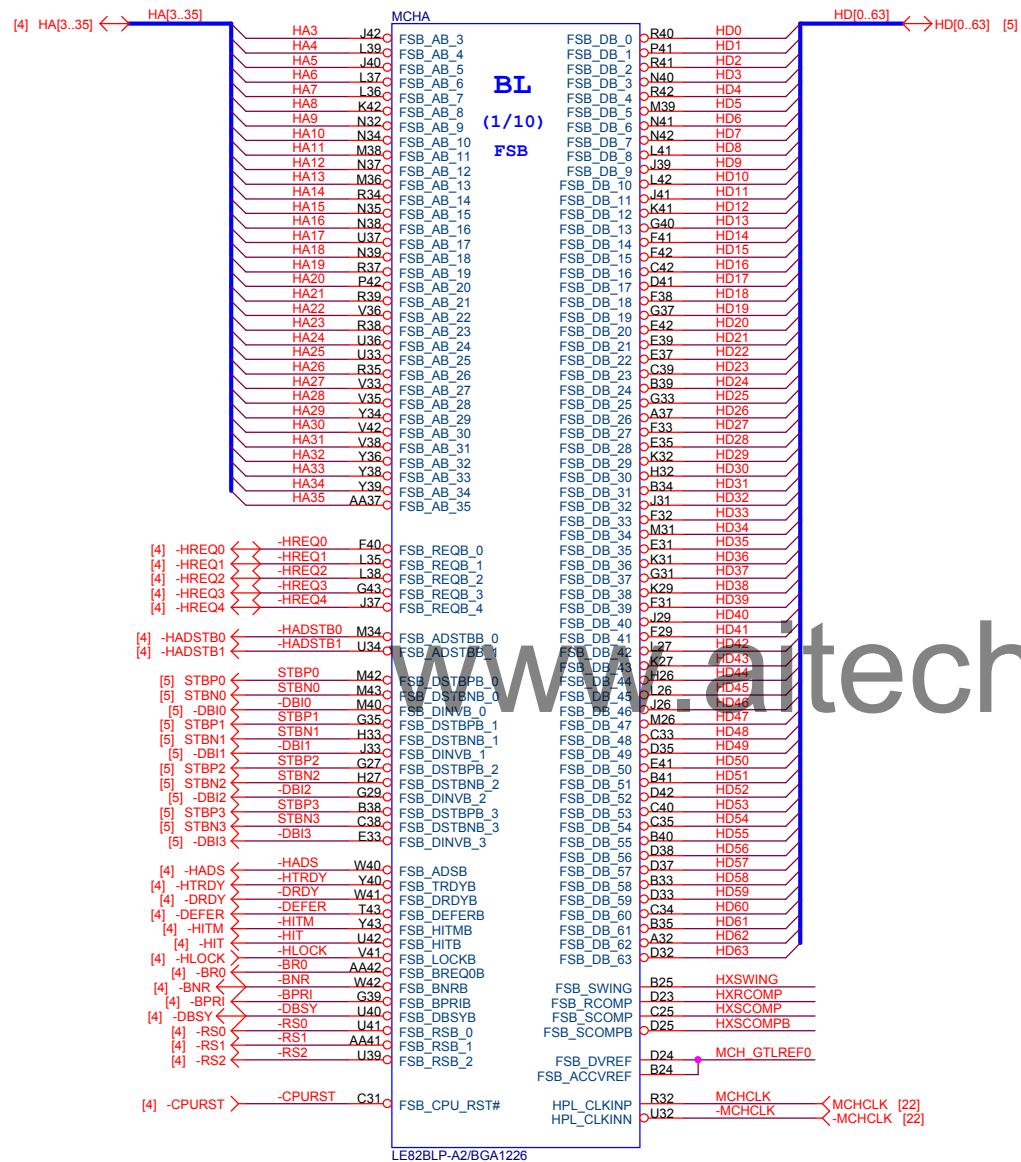


Gigabyte Technology			
P4_LGA775-C			
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PECI: Platform Environment Control Interface



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P4_LGA775-E,F,G,H			
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Gigabyte Technology

Title	GMCH-HOST		
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MCHB

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MAAA5	BB22	DDR_A_MA_5	DDR_A_DQ_0	AN3	MDA1
MAAA6	BA22	DDR_A_MA_6	DDR_A_DQ_1	AR2	MDA2
MAAA7	BB21	DDR_A_MA_7	DDR_A_DQ_2	AR3	MDA3
MAAA8	AW21	DDR_A_MA_8	DDR_A_DQ_3	AL3	MDA4
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MAAA13	AY38	DDR_A_MA_13	DDR_A_DQS1_1	AW1	DQS41
MAAA14	BA19	DDR_A_MA_14	DDR_A_DM_1	AW3	DMA1
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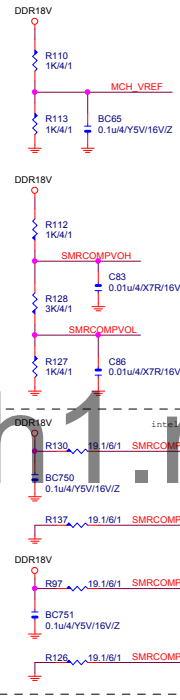
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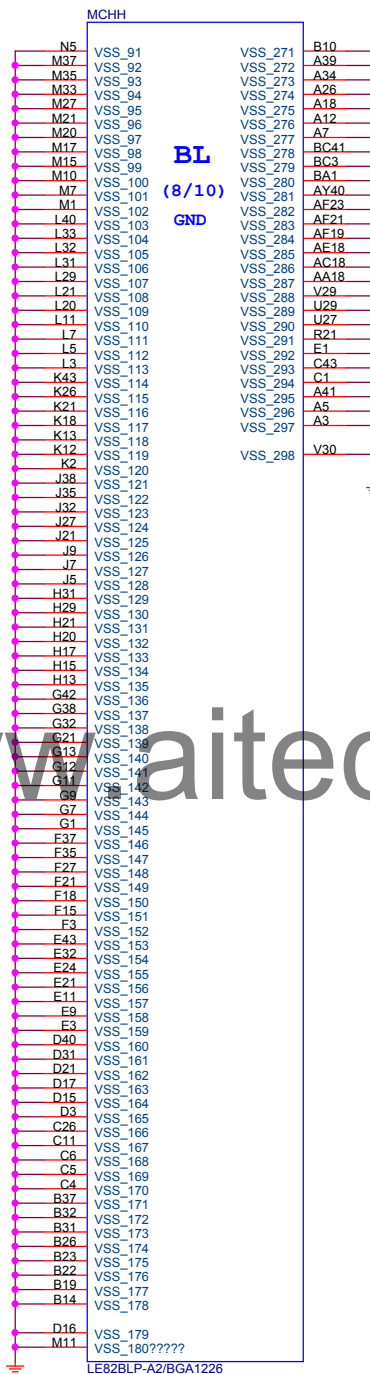
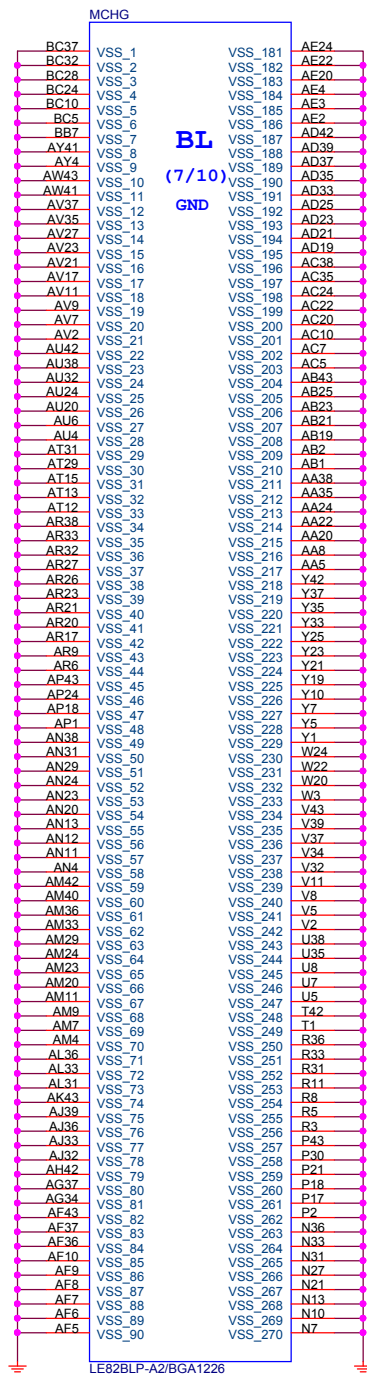
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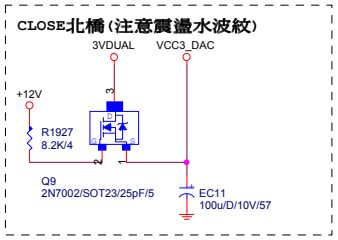
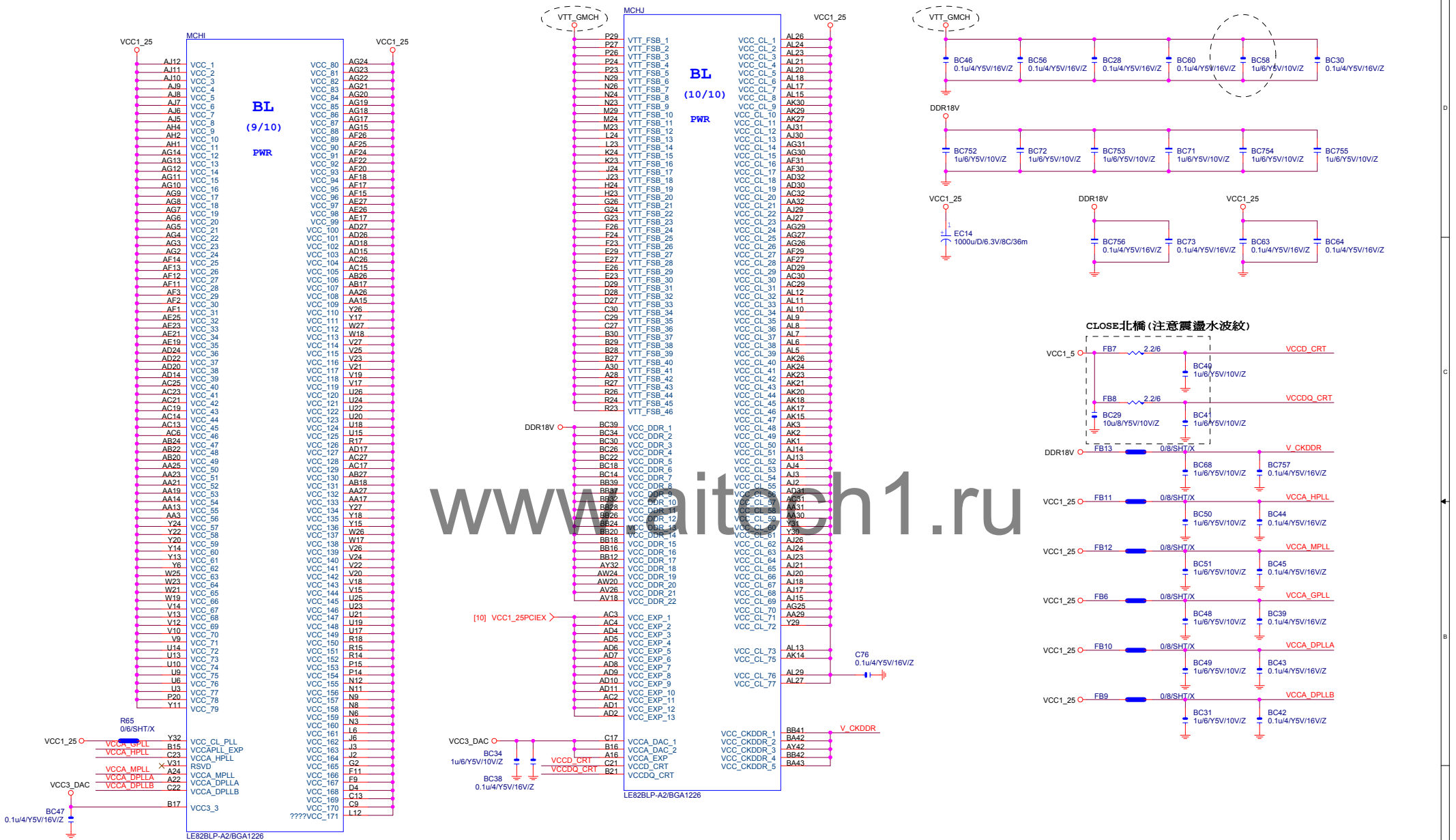
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MAAB14	BB11	DDR_B_MA_14	DDR_B_DM_1	AW9	DMA1
[16.17] -SWEB	BB25	DDR_B_WEB	DDR_B_CS0	AT11	MD88
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[16.17] -CSB14	BA30	DDR_B_CS0_14	DDR_B_DQS3_0	AU28	DQS83
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[16.17] -CSB35	BA30	DDR_B_CS0_35	DDR_B_DQS_5	AL35	DQS85
[16.17] -CSB36	BA30	DDR_B_CS0_36	DDR_B_DQS5_0	AL34	DQS85
[16.17] -CSB37	BA30	DDR_B_CS0_37	DDR_B_DM_5	AM37	DMA5
[16.17] -CSB38	BA30	DDR_B_CS0_38	DDR_B_DQ_40	AM35	MD840
[16.17] -CSB39	BA30	DDR_B_CS0_39	DDR_B_DQ_41	AM39	MD841
[16.17] -CSB40	BA30	DDR_B_CS0_40	DDR_B_DQ_42	AJ34	MD842
[16.17] -CSB41	BA30	DDR_B_CS0_41	DDR_B_DQ_43	AL38	MD843
[16.17] -CSB42	BA30	DDR_B_CS0_42	DDR_B_DQ_44	AM34	MD844
[16.17] -CSB43	BA30	DDR_B_CS0_43	DDR_B_DQ_45	AL37	MD845
[16.17] -CSB44	BA30	DDR_B_CS0_44	DDR_B_DQ_46	AL32	MD846
[16.17] -CSB45	BA30	DDR_B_CS0_45	DDR_B_DQ_47	AC35	DQS86
[16.17] -CSB46	BA30	DDR_B_CS0_46	DDR_B_DQS_6	AG35	DQS86
[16.17] -CSB47	BA30	DDR_B_CS0_47	DDR_B_DQS6_0	AG39	DMA6
[16.17] -CSB48	BA30	DDR_B_CS0_48	DDR_B_DQ_48	AG38	MD848
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[16.17] -CSB50	BA30	DDR_B_CS0_50	DDR_B_DQ_50	AF35	MD850
[16.17] -CSB51	BA30	DDR_B_CS0_51	DDR_B_DQ_51	AF33	MD851
[16.17] -CSB52	BA30	DDR_B_CS0_52	DDR_B_DQ_52	AJ37	MD852
[16.17] -CSB53	BA30	DDR_B_CS0_53	DDR_B_DQ_53	AJ35	MD853
[16.17] -CSB54	BA30	DDR_B_CS0_54	DDR_B_DQ_54	AC33	MD854
[16.17] -CSB55	BA30	DDR_B_CS0_55	DDR_B_DQ_55	AF34	MD855
[16.17] -CSB56	BA30	DDR_B_CS0_56	DDR_B_DQS_7	AC36	DQS87
[16.17] -CSB57	BA30	DDR_B_CS0_57	DDR_B_DQS7_0	AC37	DQS87
[16.17] -CSB58	BA30	DDR_B_CS0_58	DDR_B_DM_7	AD38	DMA7
[16.17] -CSB59	BA30	DDR_B_CS0_59	DDR_B_DQ_56	AD36	MD856
[16.17] -CSB60	BA30	DDR_B_CS0_60	DDR_B_DQ_57	AC33	MD857
[16.17] -CSB61	BA30	DDR_B_CS0_61	DDR_B_DQ_58	AD34	MD858
[16.17] -CSB62	BA30	DDR_B_CS0_62	DDR_B_DQ_59	AD36	MD859
[16.17] -CSB63	BA30	DDR_B_CS0_63	DDR_B_DQ_60	AD34	MD860
[16.17] -CSB64	BA30	DDR_B_CS0_64	DDR_B_DQ_61	AD38	MD861
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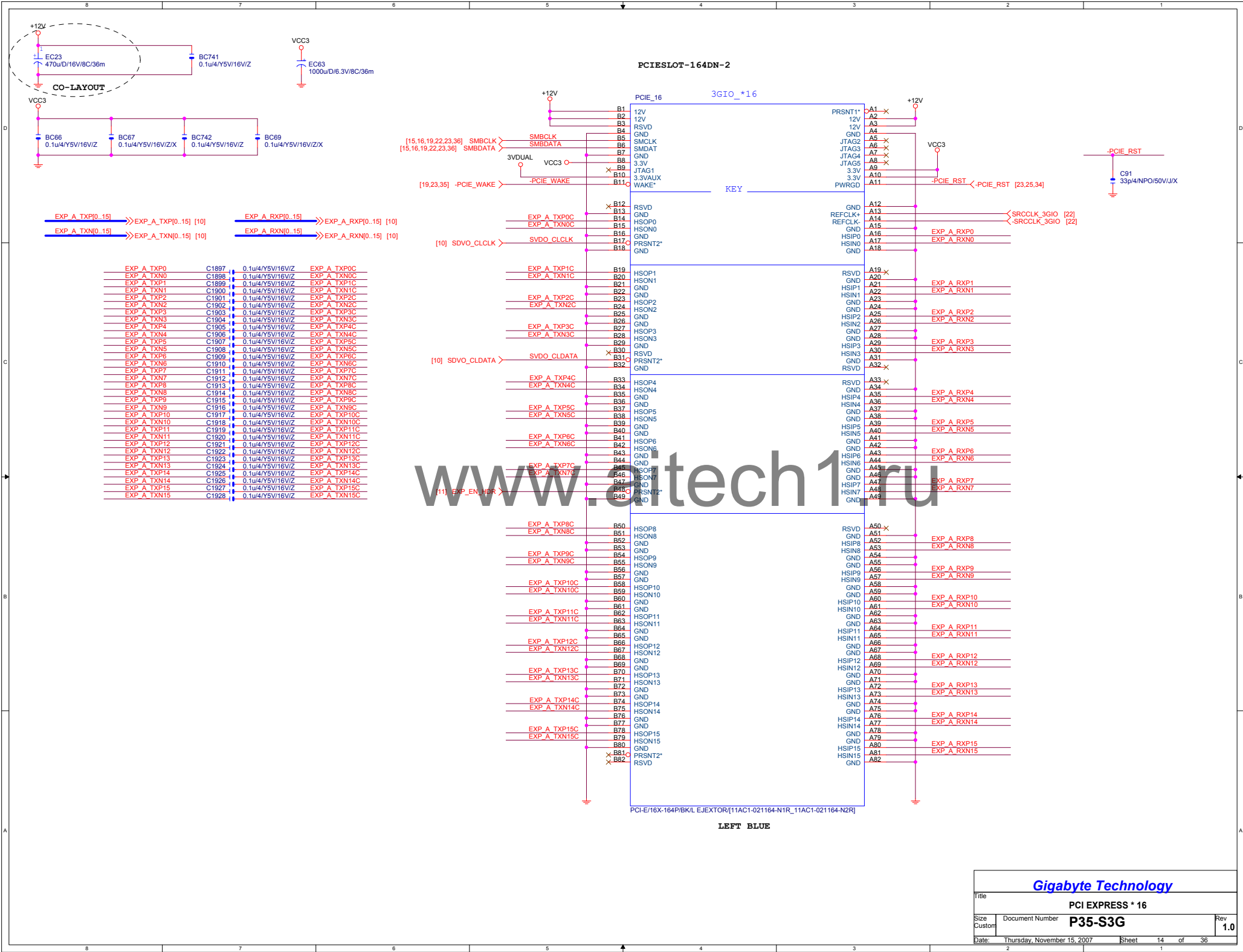
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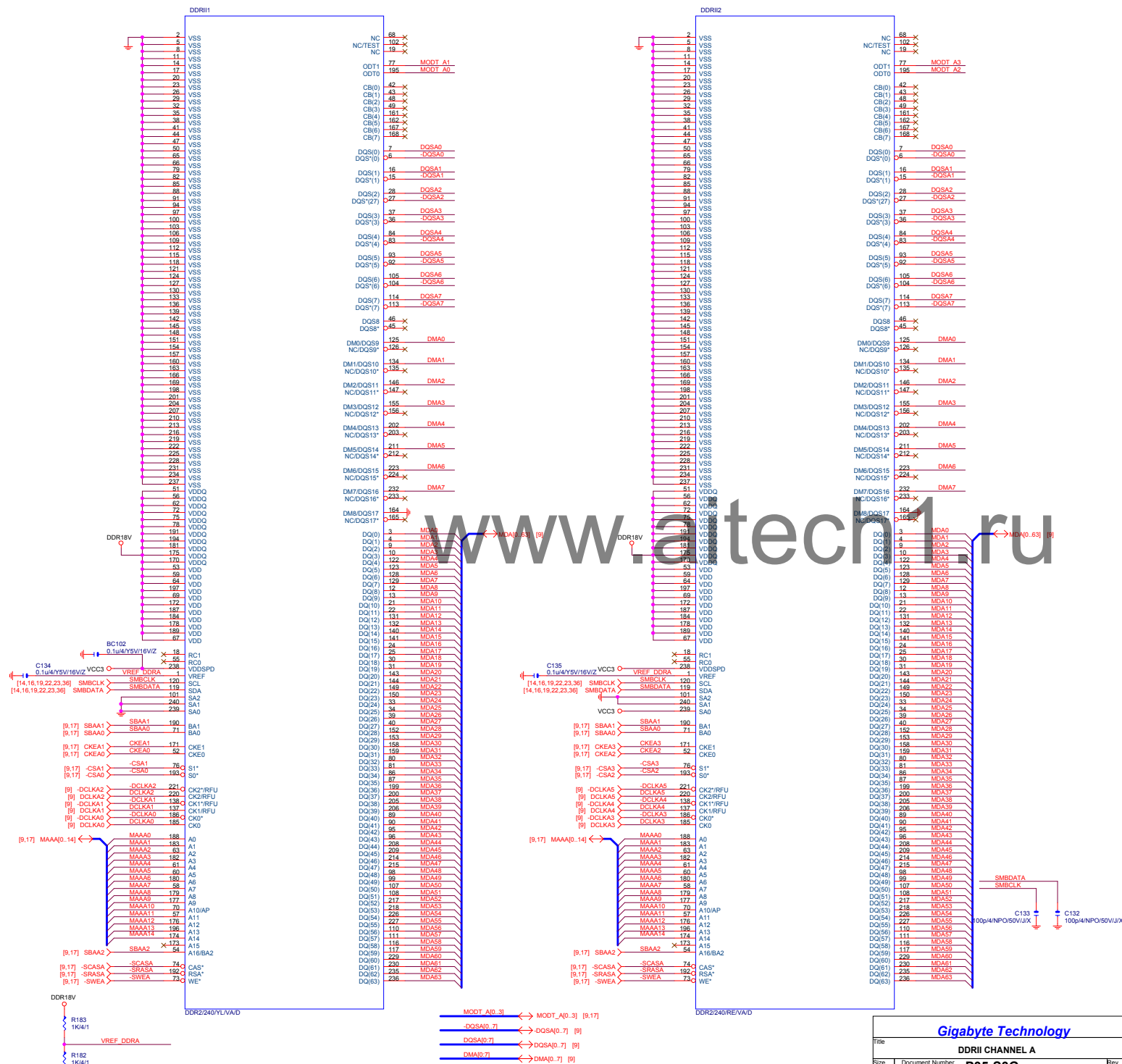
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[16.17] MODT_B0_3]	MODT_B0_3]
[16] -DQS0_7]	-DQS0_7]
[16.17] MAAB0_14]	MAAB0_14]
[16] DMB0_7]	DMB0_7]
[16] MDB0_63]	MDB0_63]
[16] DQS0_7]	DQS0_7]
[15.17] MAAB0_14]	MAAB0_14]
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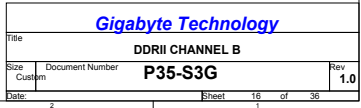






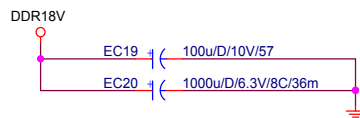
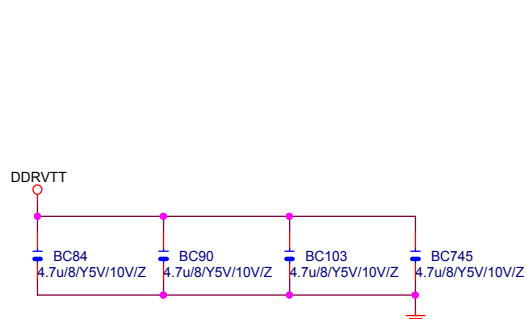




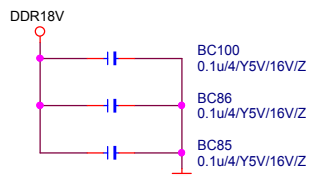


DDR TERMINATION CHANNEL A

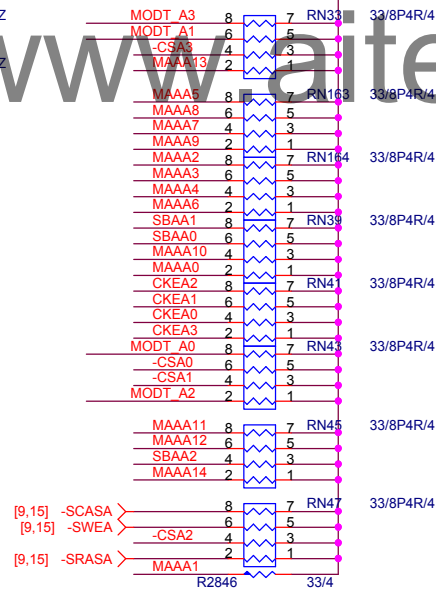
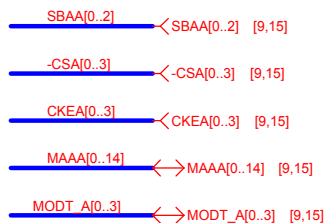
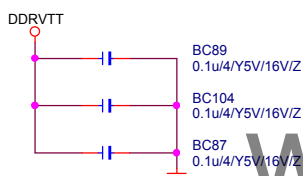
DDRVTT Decouple



DDR18V Decouple

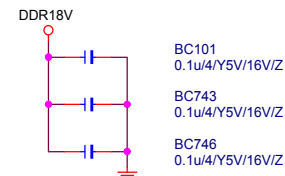


DDRVTT Decouple

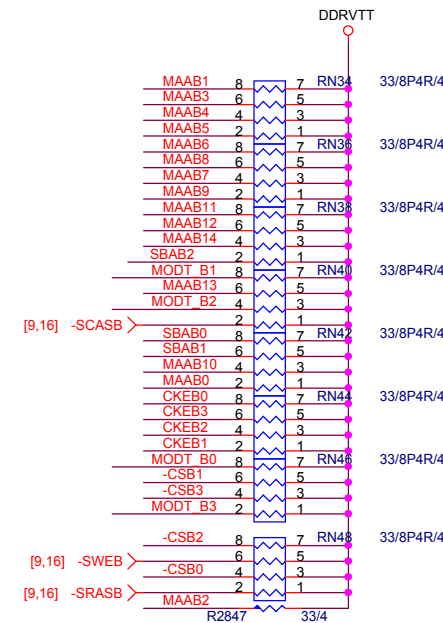
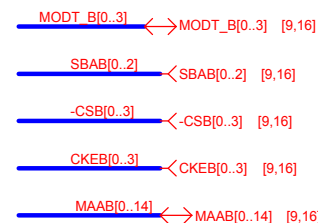
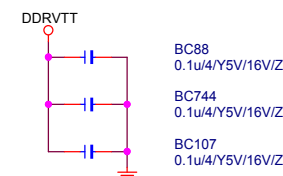


DDR TERMINATION CHANNEL B

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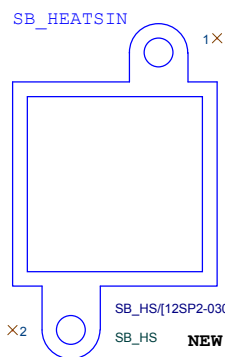


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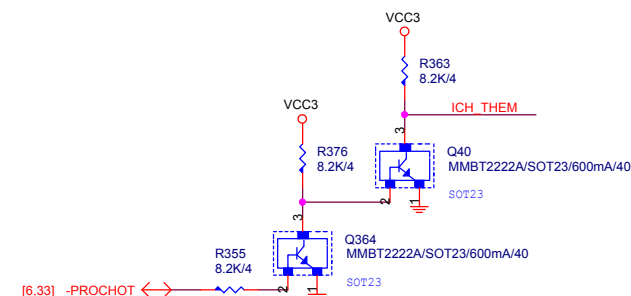
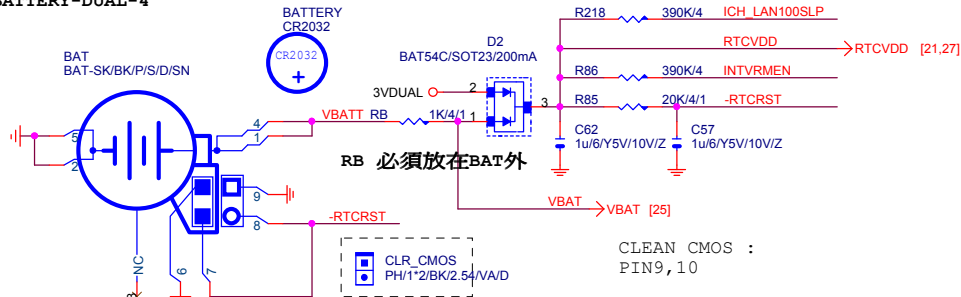
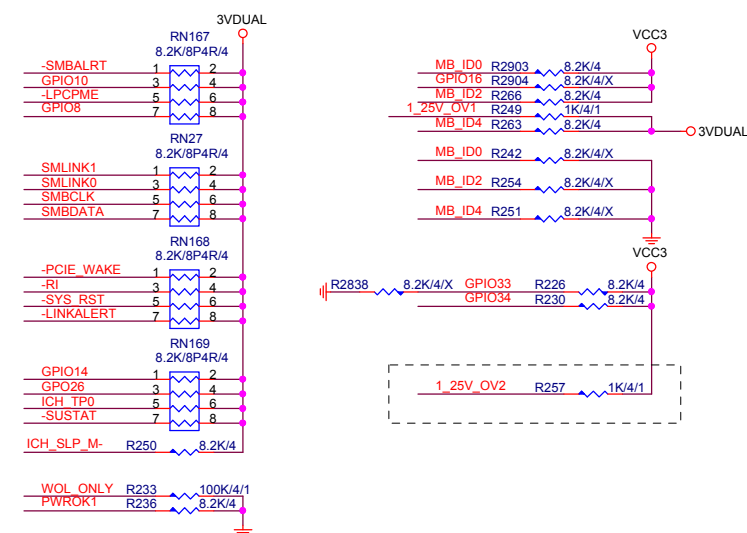


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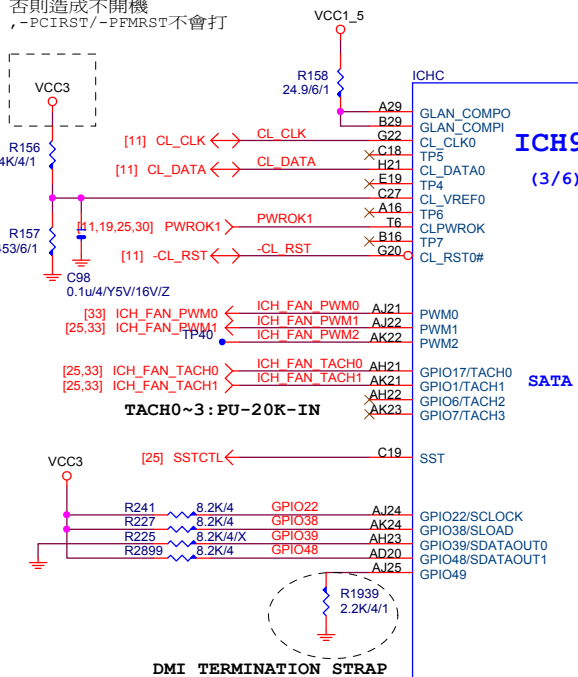
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DDRII TERMINATOR			
Size	Document Number	P35-S3G	
Custom			Rev 1.0
Date:	Thursday, November 15, 2007	Sheet 17	of 36



SB_HS NEW SB HS 對邊 (GOLD)



修改成VCC3，
否則造成不開機
，-PCIRST/-PFMRST不會打



ICH9
(3/6)

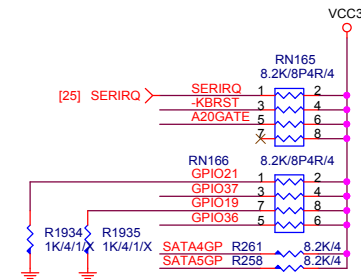
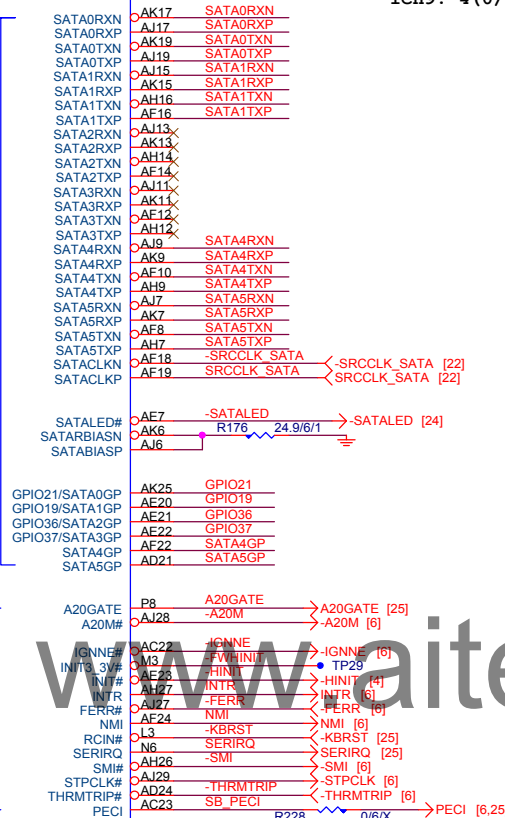
SATA

HOST

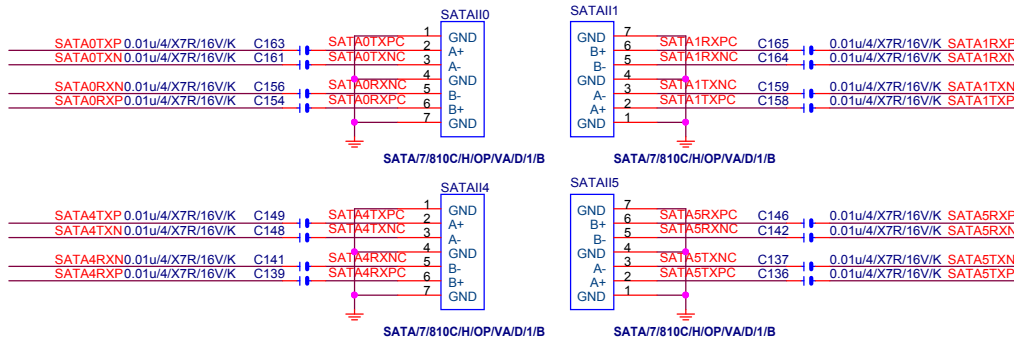
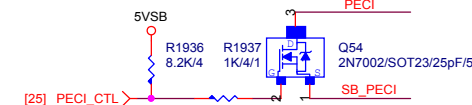
NH82801B-A2/BGA676/[10HB1-038280-90R]

INTEL NOTE:SATAII PORT

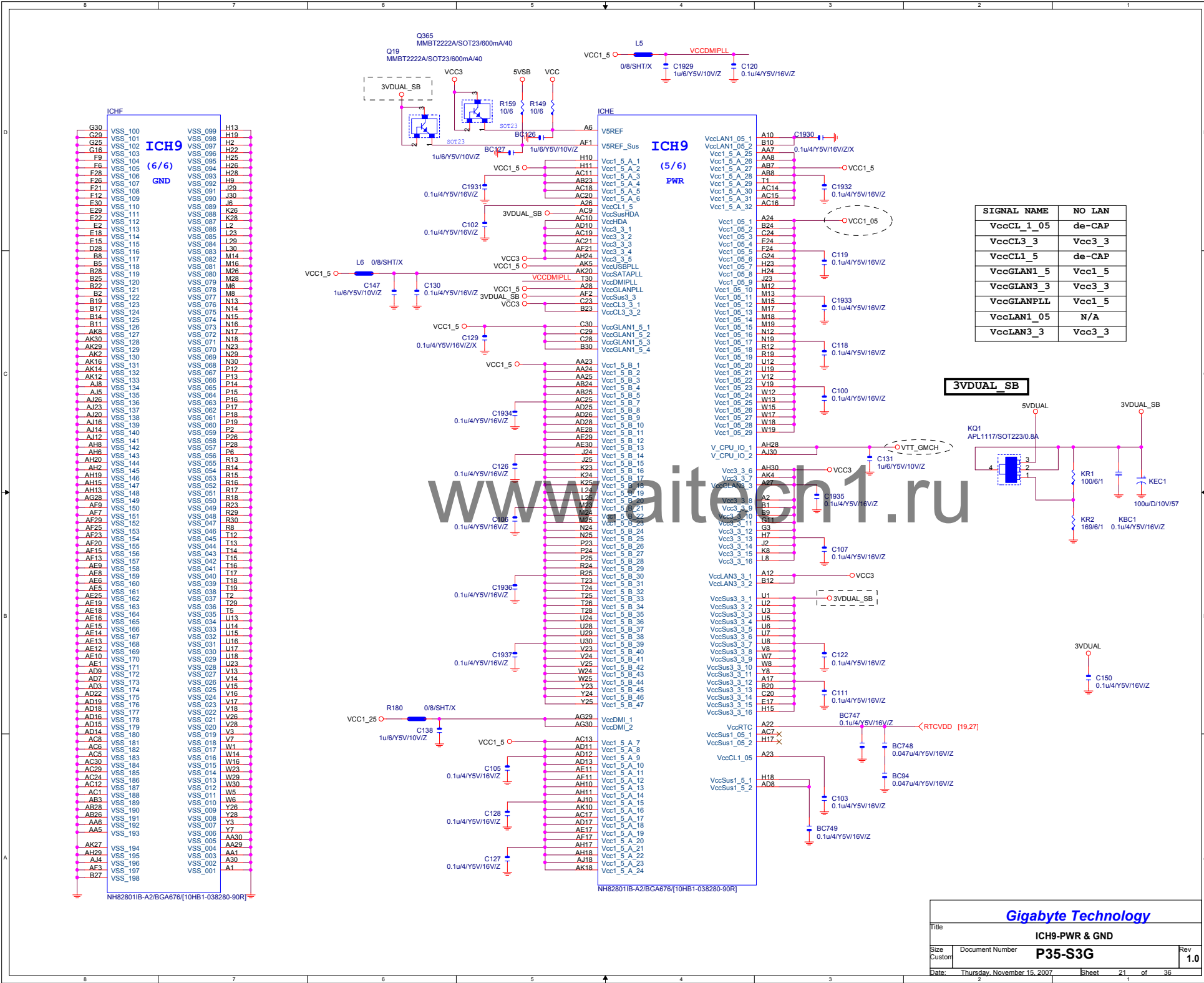
ICH9: 4 (0/1/4/5 PORT,2/3:N/A)

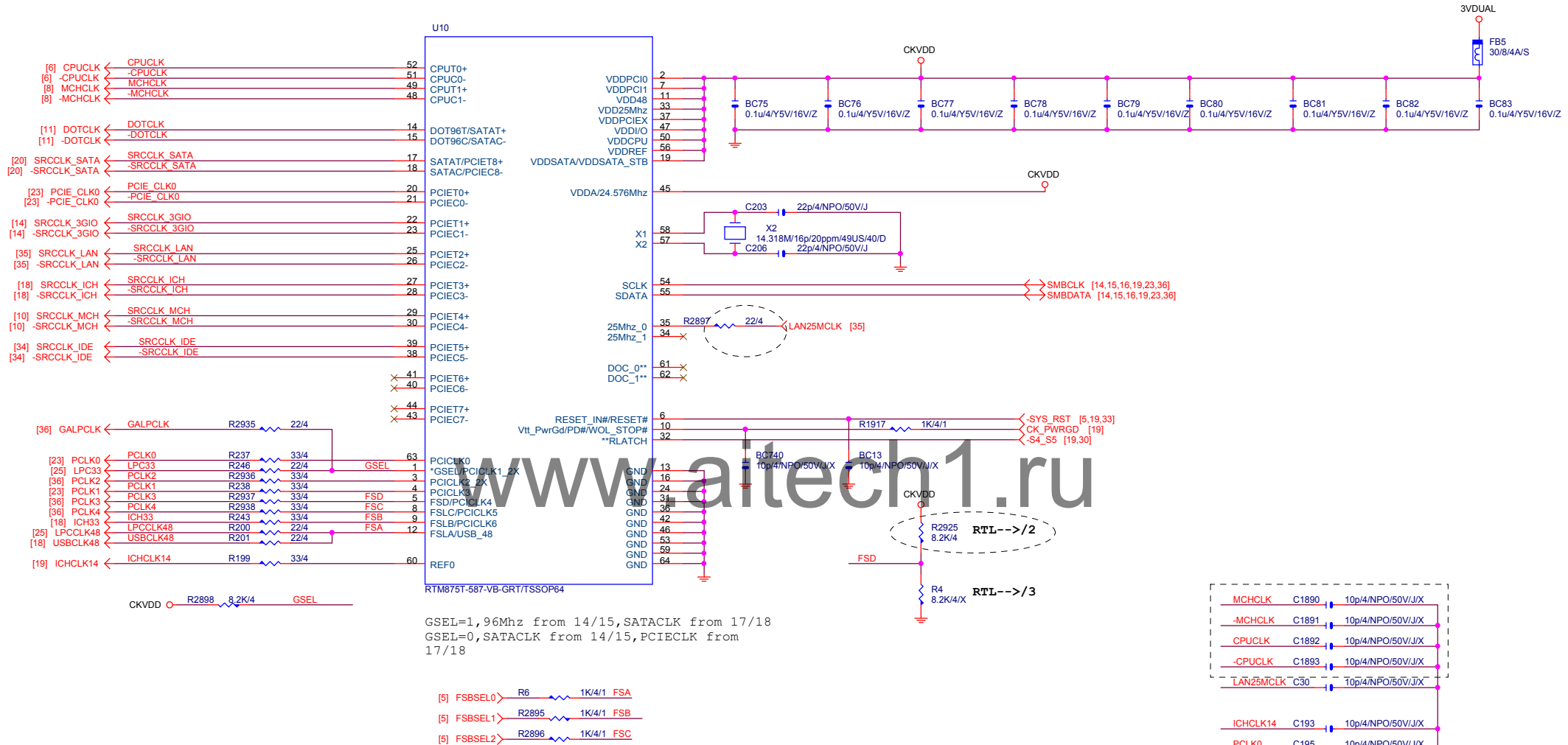


FOR ICH8 PECI



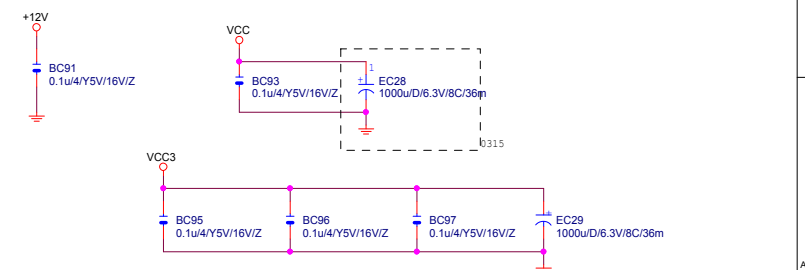
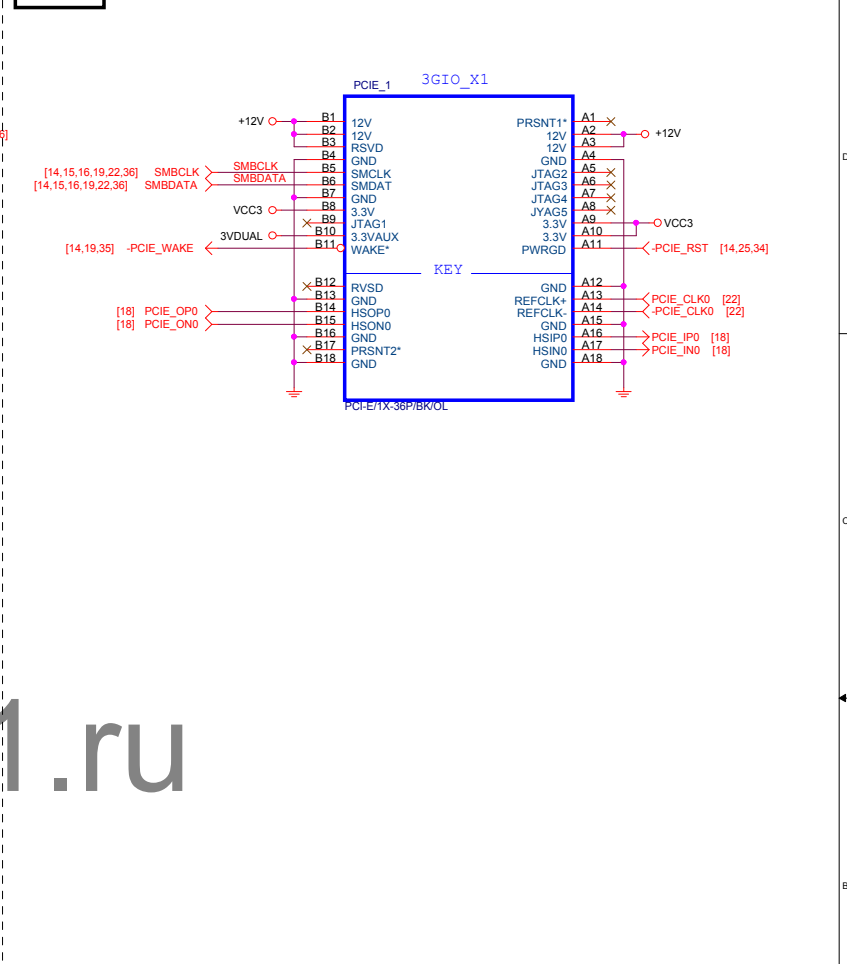
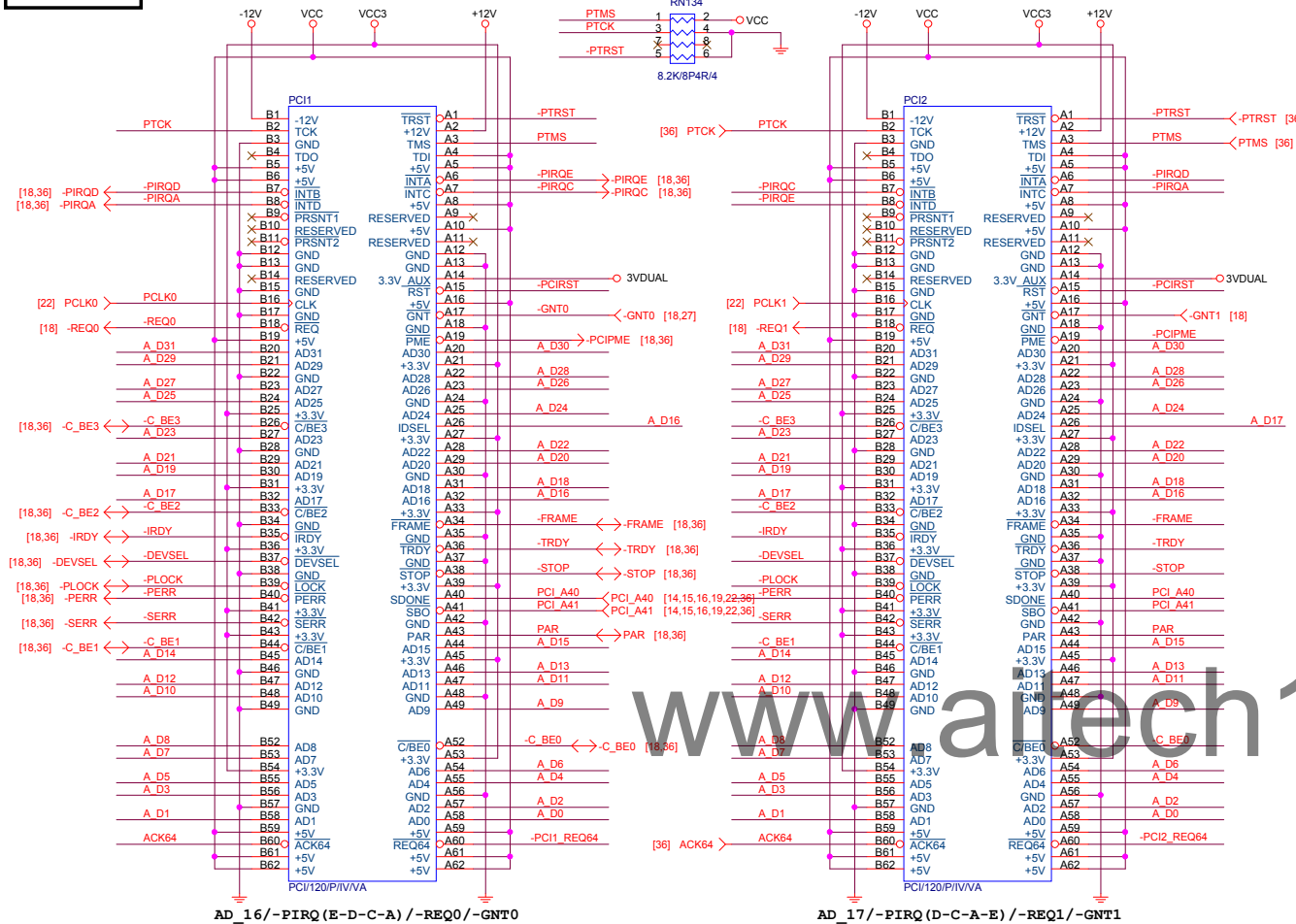
Gigabyte Technology



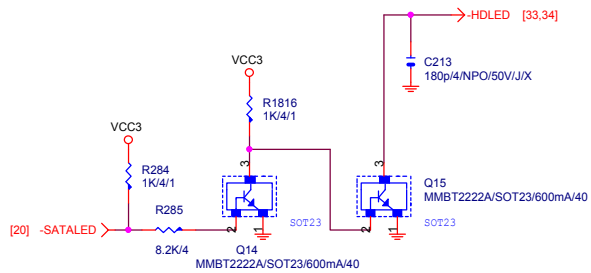


Gigabyte Technology

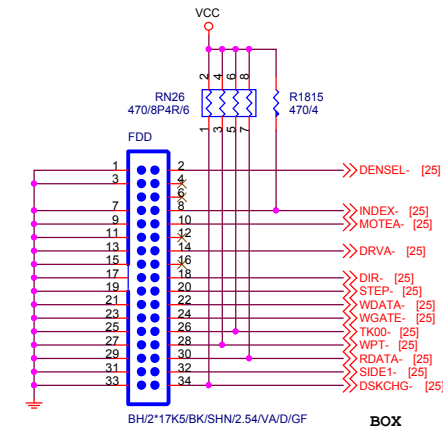
Title			CK505 CLK GEN		
Size			P35-S3G		
Custom			Rev 1.0		
Date:	Thursday, November 15, 2007	Sheet	22	of	36



IDE/SATA LED



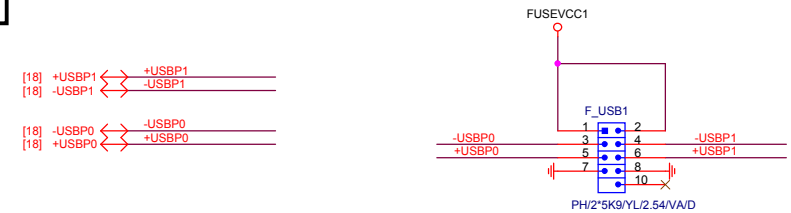
FLOPPY



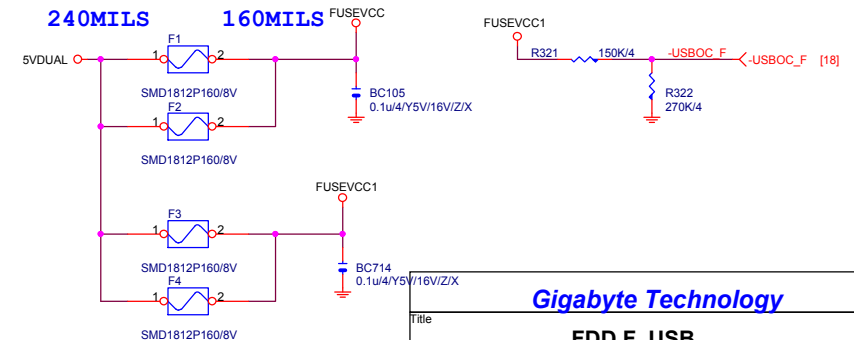
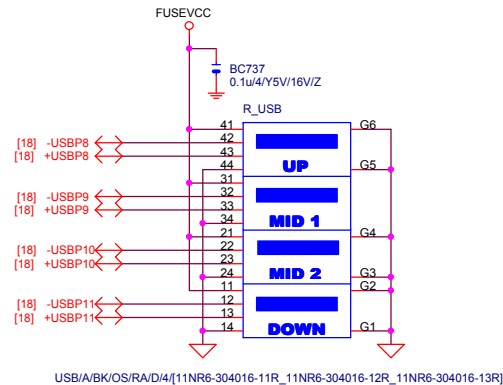
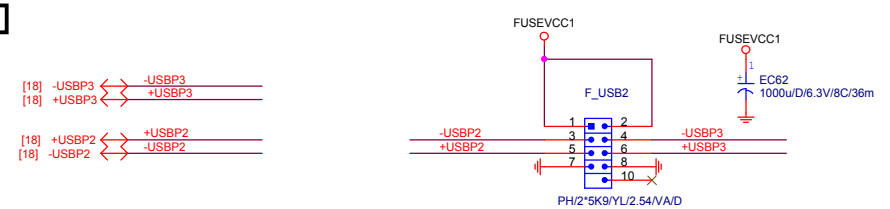
FRONT USB3



FRONT USB1



FRONT USB2



Gigabyte Technology

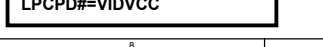
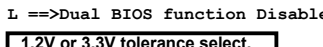
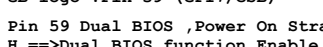
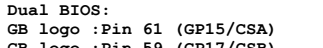
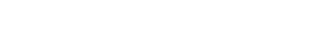
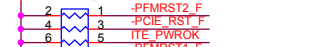
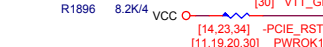
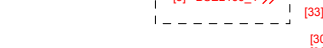
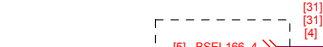
Title		
FDD,F_USB		
Size	Document Number	Rev
B	P35-S3G	1.0
Date: Thursday, November 15, 2007		
Sheet 24 of 36		

RTS2- ==LOW CPU FAN 50%
==HIGH 100%

DEFAULT 50%



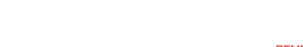
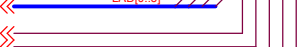
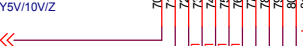
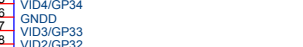
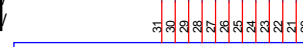
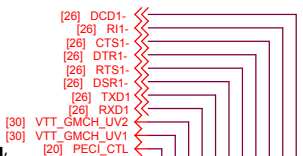
SOUT2 1 VID pins threshold voltage select: Vih / Vil : 2.0 / 0.8
0 VID pins threshold voltage select: Vih / Vil : 0.8 / 0.4



Dual BIOS:
GB logo :Pin 61 (GP15/CSA)
GB logo :Pin 59 (GP17/CSB)

Pin 59 Dual BIOS ,Power On Strapping:
H ==>Dual BIOS function Enable
L ==>Dual BIOS function Disable

1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接 3.3V
LPCPD# =VIDVCC



IT8712F/[IT8718F]

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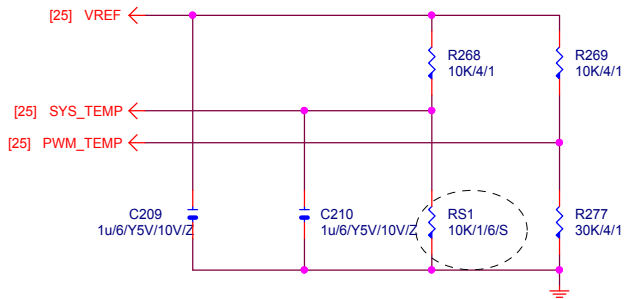
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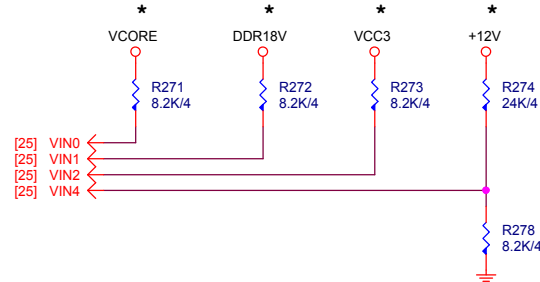
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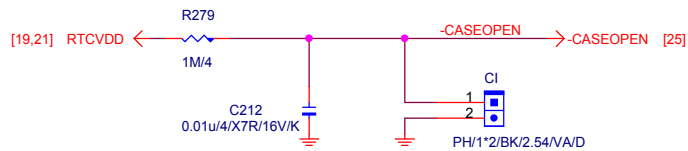
TEMP H/W MONITOR



VOLTAGE-- H/W MONITOR

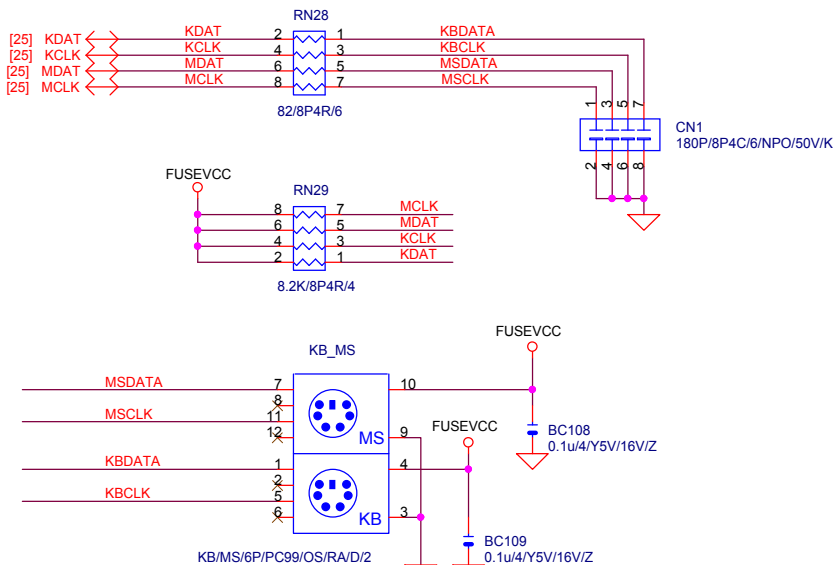


CASE OPEN

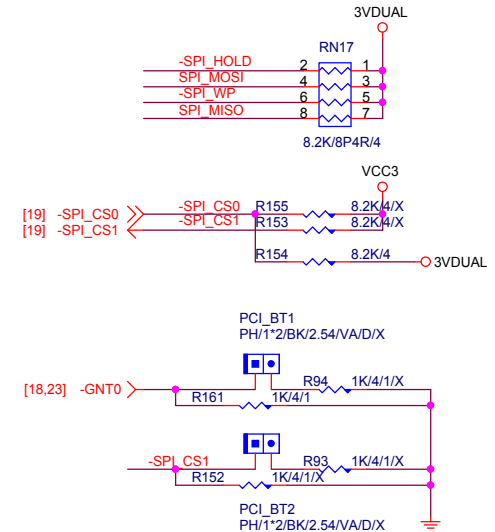
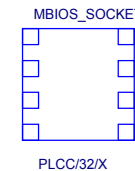
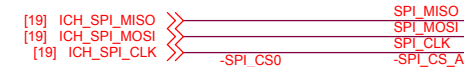
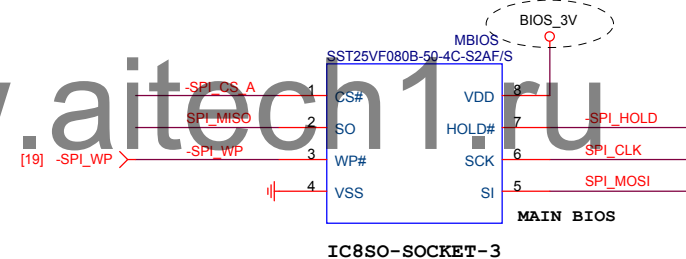
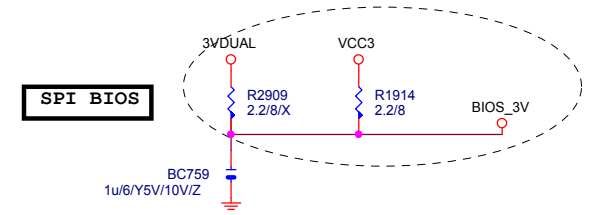


Case Open Circuits

KB/MS



SPI BIOS



BOOT DEVICE	GNT0	CS1
SPI	0	1
PCI	1	0
FWH	1	1

Gigabyte Technology

HW-MONITOR/CI/KB/MS/BIOS

Size	Document Number	Rev
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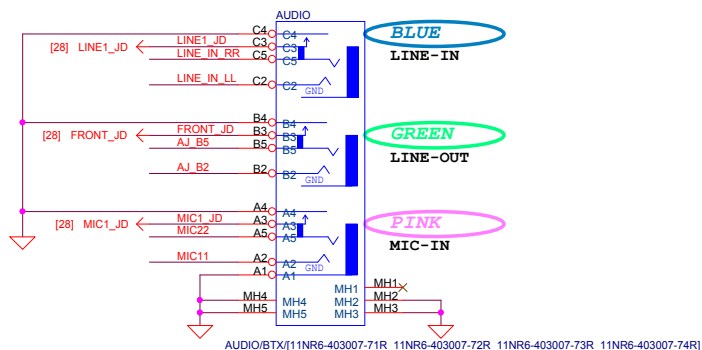
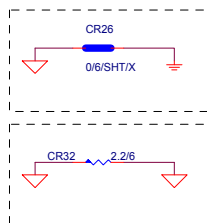
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Figure 10 is a schematic diagram of the output filter. It shows two input lines, [28] LINE_O_R and [28] LINE_O_L, each connected to a common-mode choke (CR104 and CR105, 10uS/16V/45) and a series resistor (75.6/1). The lines then pass through a common-mode choke (CR106, 22K/4) and a series resistor (22K/4) before being connected to the output filter capacitors (CBC21 and CBC22, 180p4/NPO/50V/J). The output filter is connected to the output lines AJ_B5 and AJ_B2.

[28] LINE_IN_R ← CR108 75.6/1

[28] LINE_IN_L ← CR109 75.6/1

CR110 22K/4

CR111 22K/4

180p4/NPO/50V/J

CBC26

CBC27 180p4/NPO/50V/J

[28] VREFO_32 >

[28] VREFO_28 >

[28] MIC2 <

[28] MIC1 <

CR112 2.2K/4/1

CR113 2.2K/4/1

CR114 75/6/1

CR115 75/6/1

CR116 22K/4

CR117 22K/4

CBC28 180p/4/NPO/50V/J

CBC29 180p/4/NPO/50V/J

MIC22

MIC11

AZALIA FRONT PANEL

QO8 BAT54A/SOT23/200mA

[28] LINE2_VREFO

QO9 BAT54A/SOT23/200mA

[28] MIC2_VREFO

[28] MIC2_L

[28] MIC2_R

[28] LINE2_L

CEC9 100uD/10V/57

CEC10 100uD/10V/57

CR74 8.2K/4

CR75 8.2K/4

CR76 8.2K/4

CR77 8.2K/4

CR118 22K/4

CR119 22K/4

CR97 22K/4

CR98 22K/4

CR120 75/6/1

CR121 75/6/1

CR99 75/6/1

CR100 75/6/1

CR78 8.2K/4

CR79 20K/4/1

CR80 39.2K/4/1

PH2*5K/GED/2.54/VA/D

CBC45 4.7u/8/Y5V/10V/Z

CBC44 4.7u/8/Y5V/10V/Z

CBC46 180p/4/NPO/50V/J

CBC47 180p/4/NPO/50V/J

CBC48 180p/4/NPO/50V/J

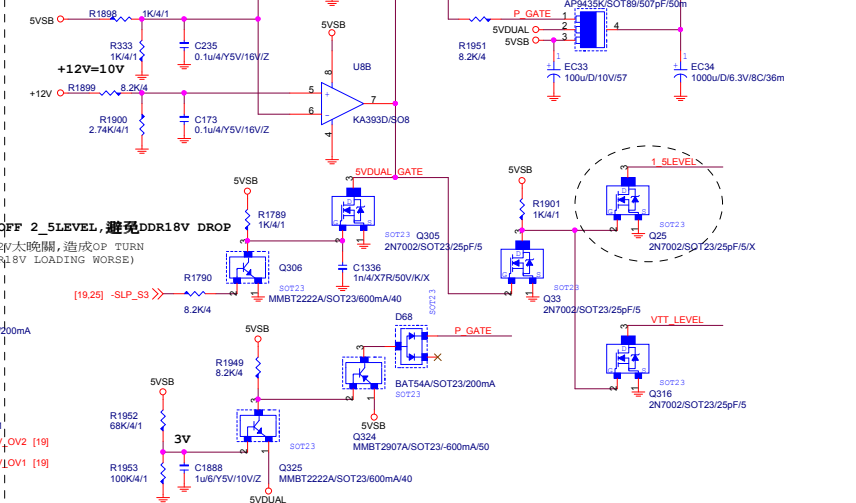
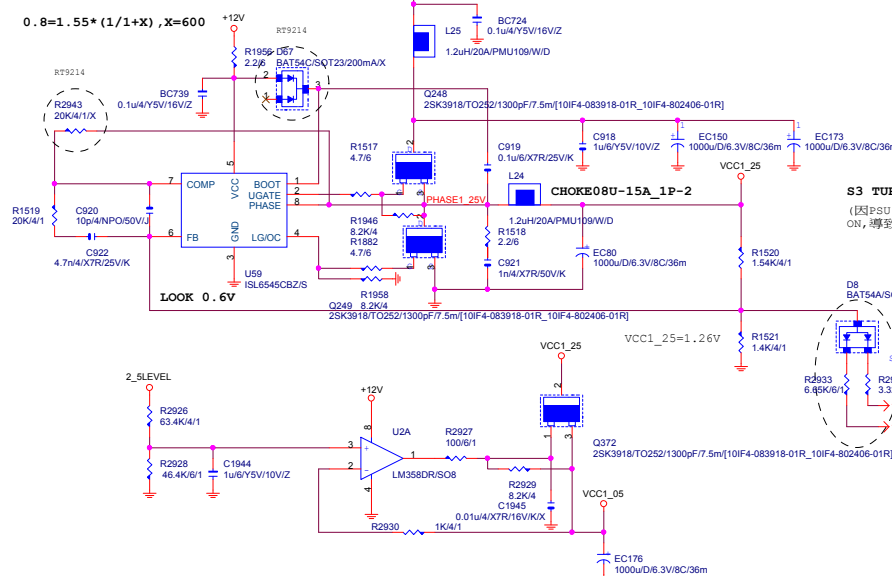
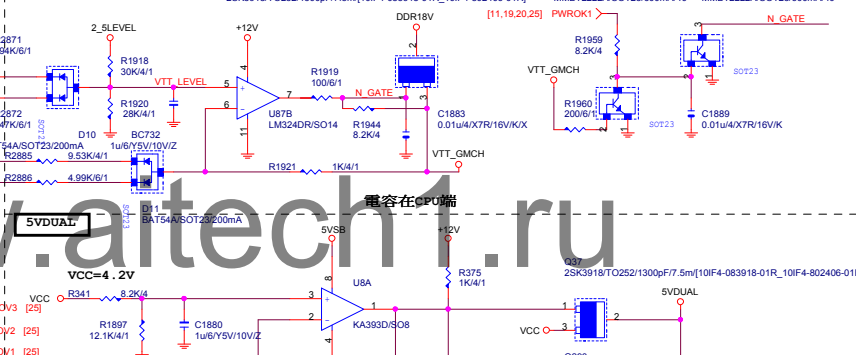
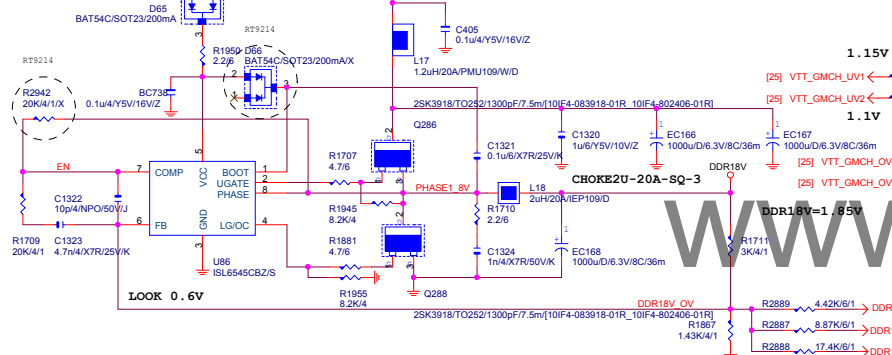
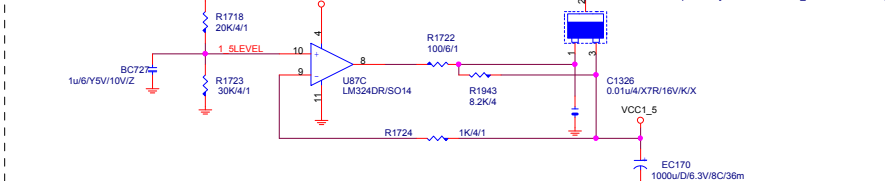
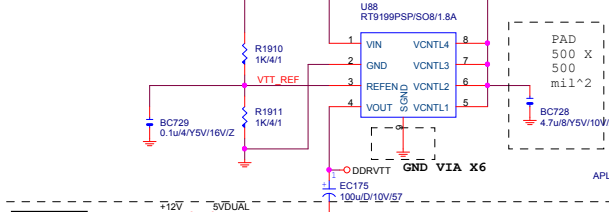
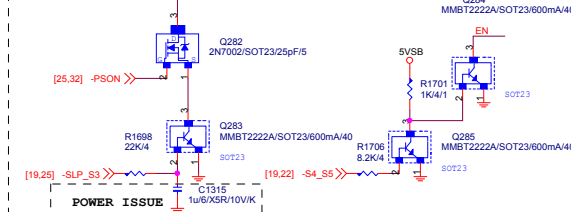
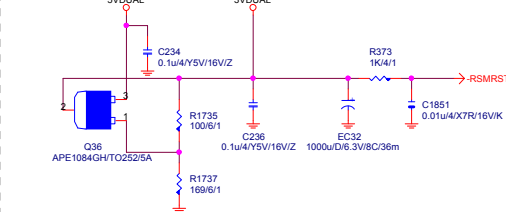
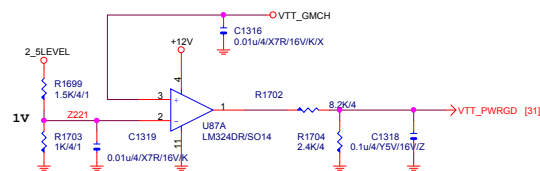
CBC49 180p/4/NPO/50V/J

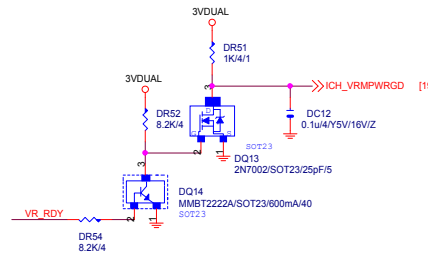
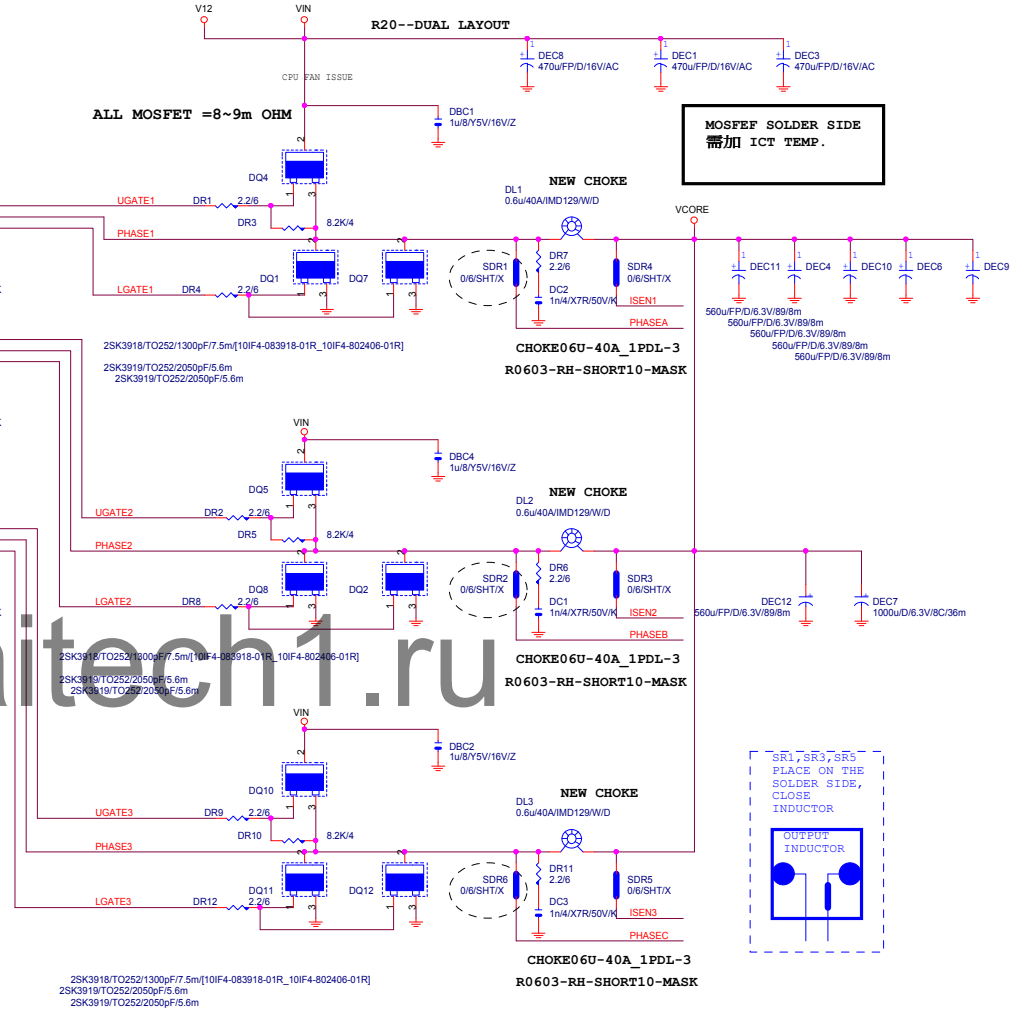
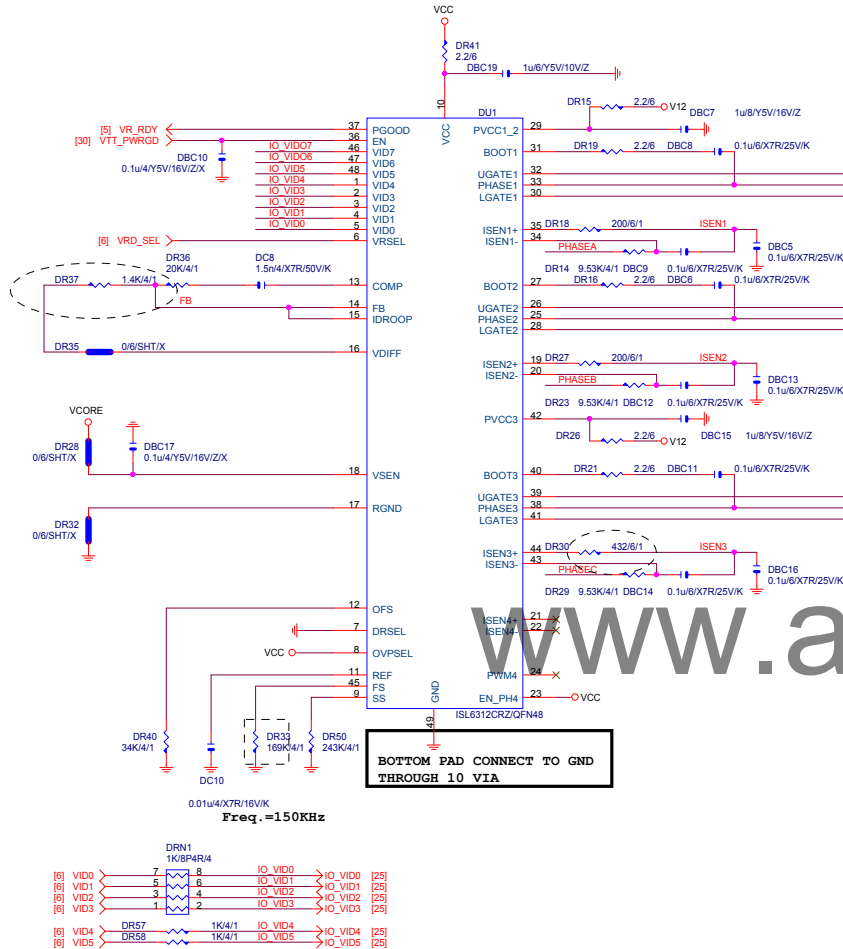
F_AUDIO

VCC3

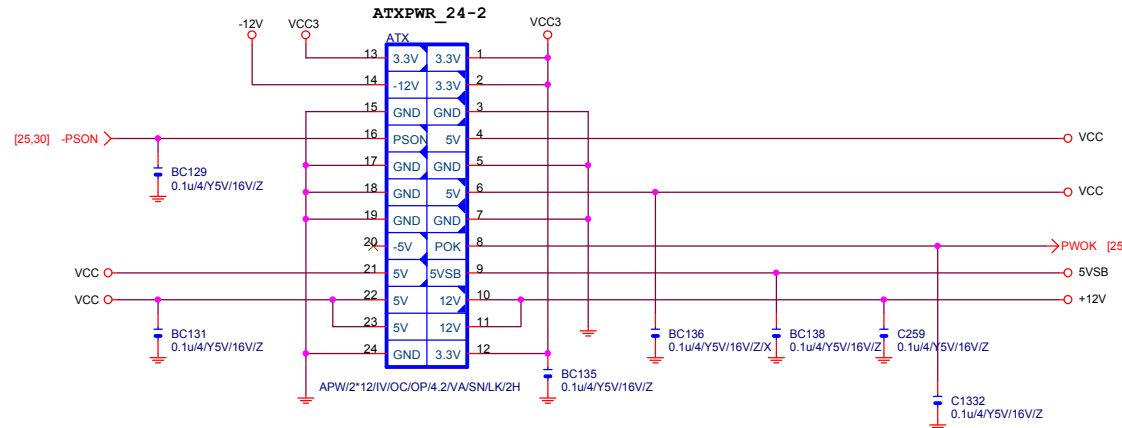
ACZ_DET [19,28]

FAUDIO_ID [28]

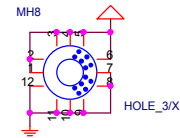
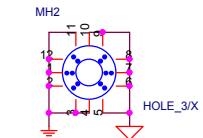
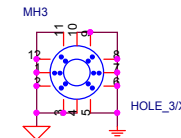
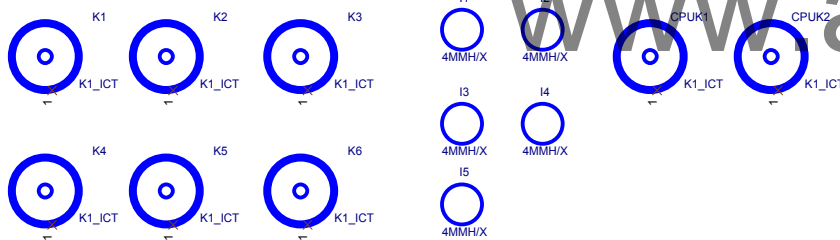
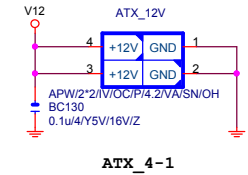
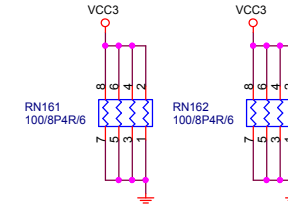




ATX POWER CONNECTOR

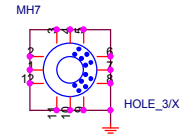
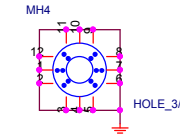
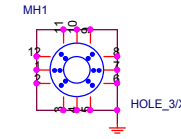
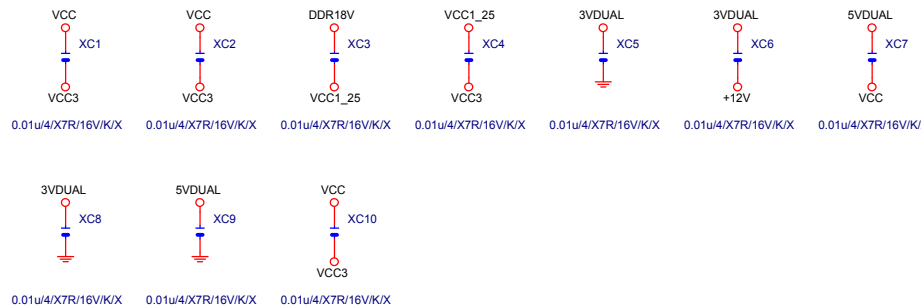


FIX PWR AcBel (ATX-400C-A2ADB)



HOLE_4-RH

HOLE_4-RH-5MM



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ATX POWER CONNECTOR

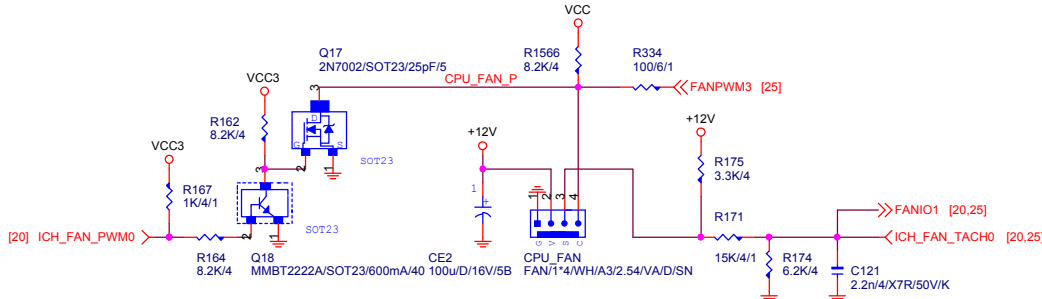
P35-S3G

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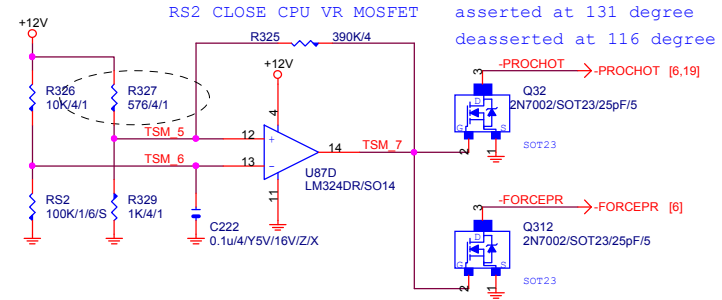
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CPU SMART FAN

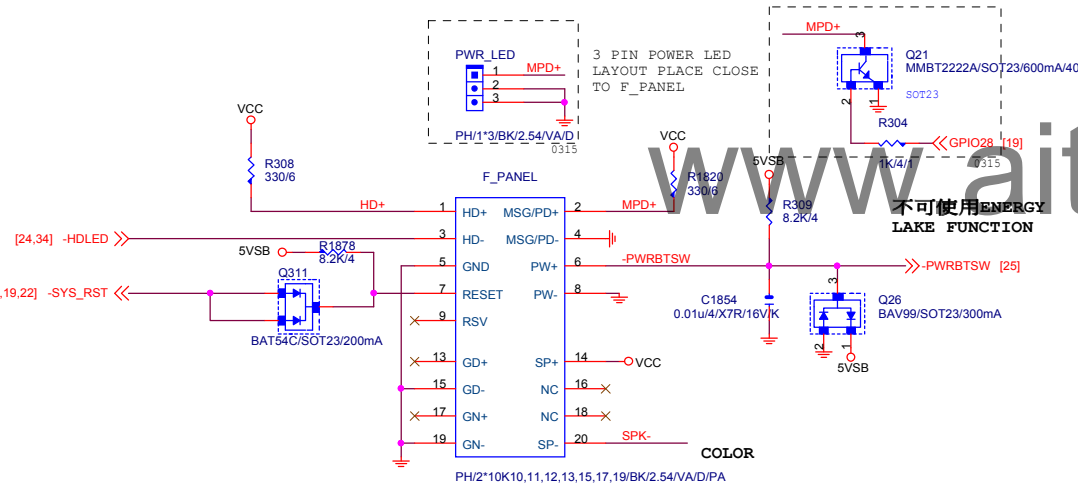
SMART FAN



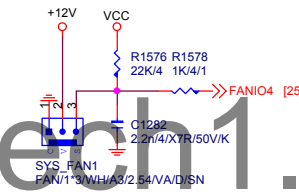
PROCESSOR HOT



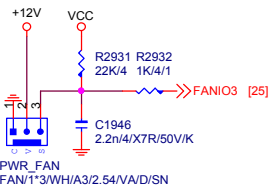
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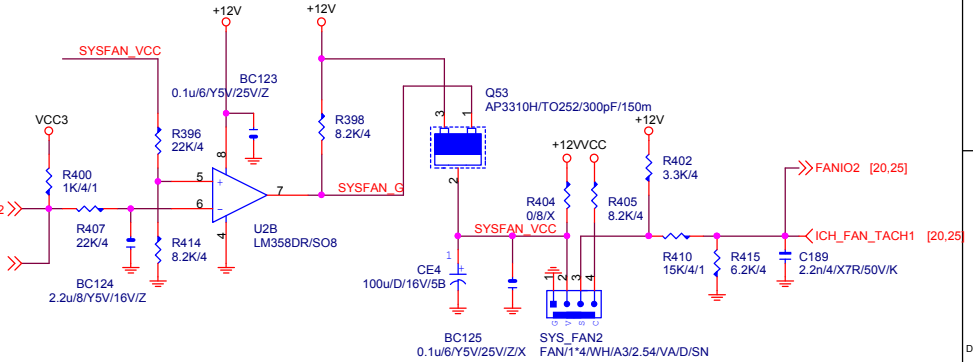
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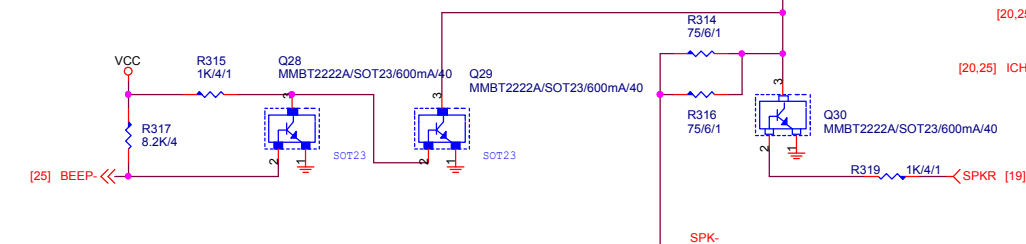
PWR_FAN



SYS SMART FAN



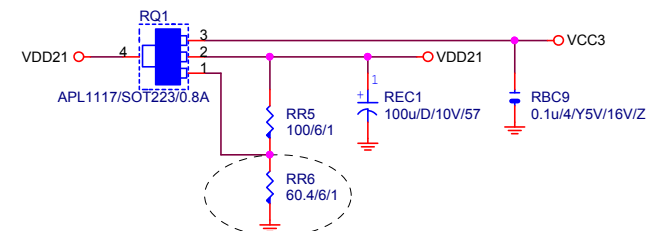
BUZZER



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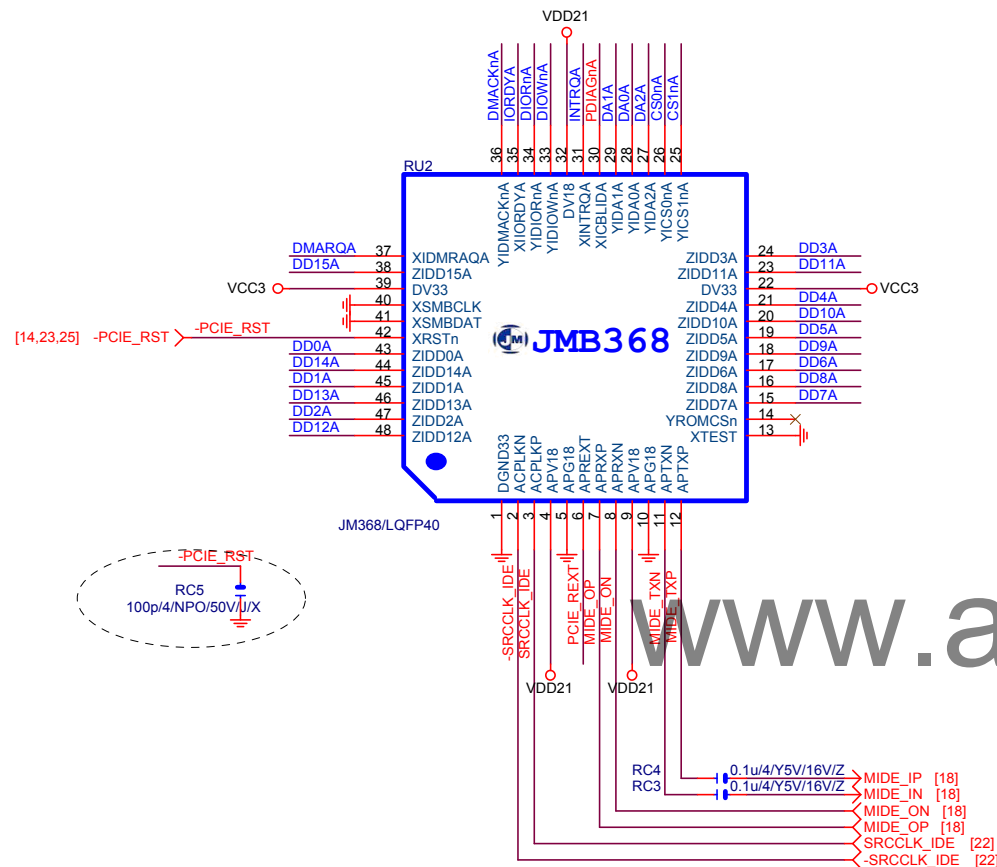
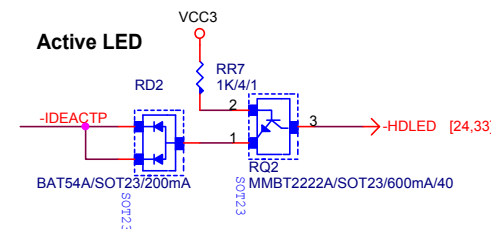
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3.3V to 2.1V Voltage Regulator



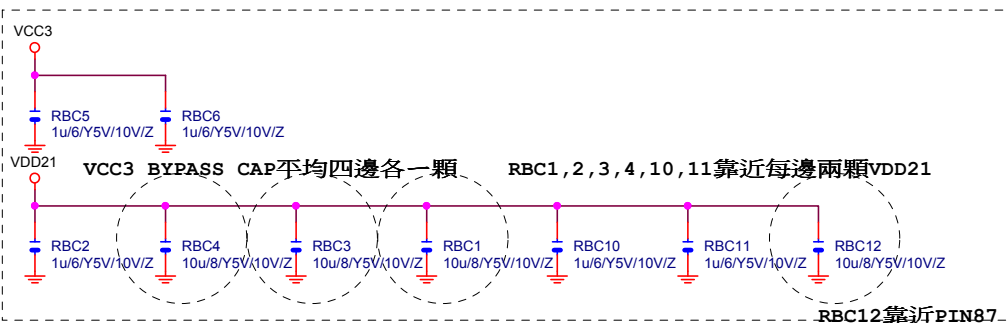
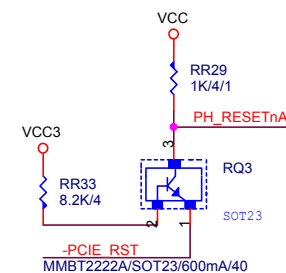
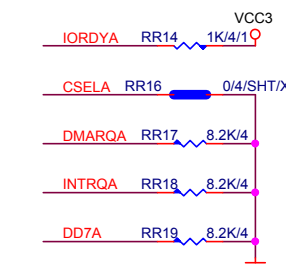
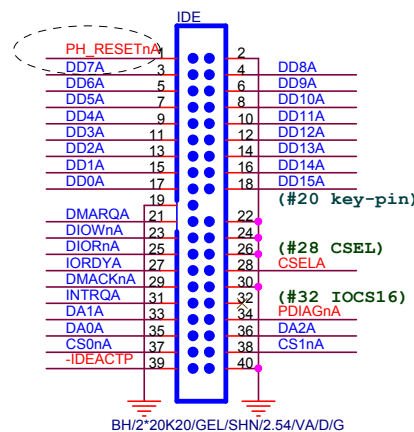
JMicron suggest JMB368 to 2.1V

Active LED

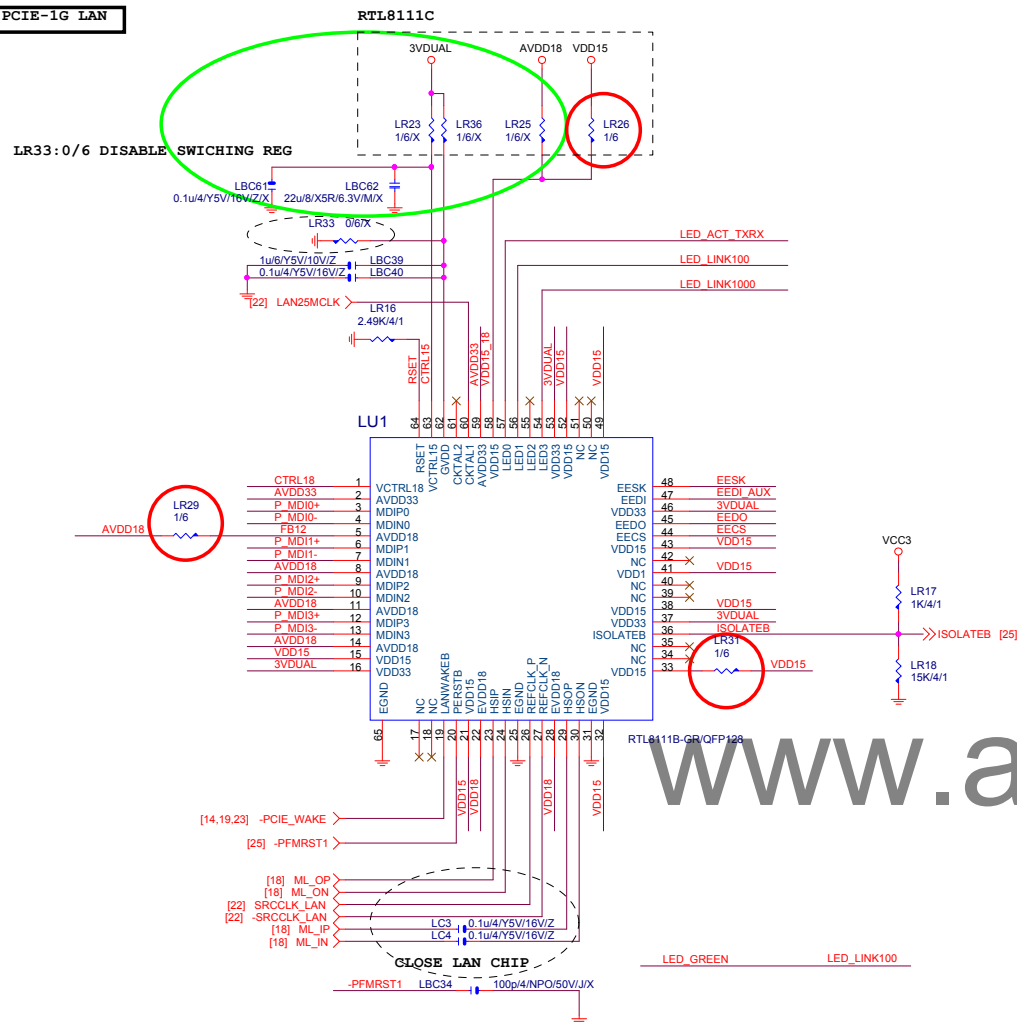


IDE Connector

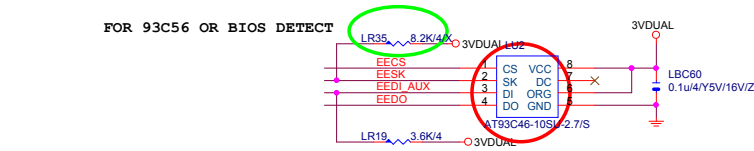
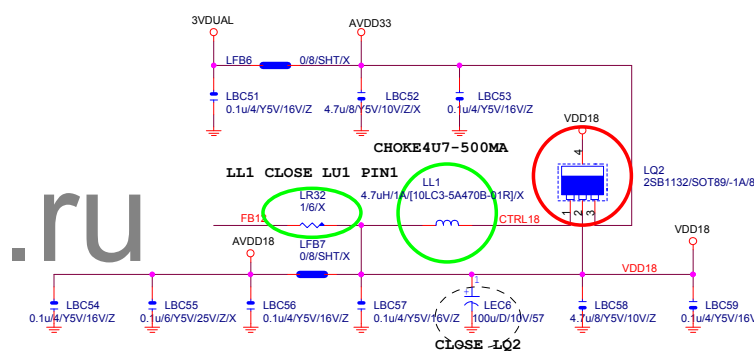
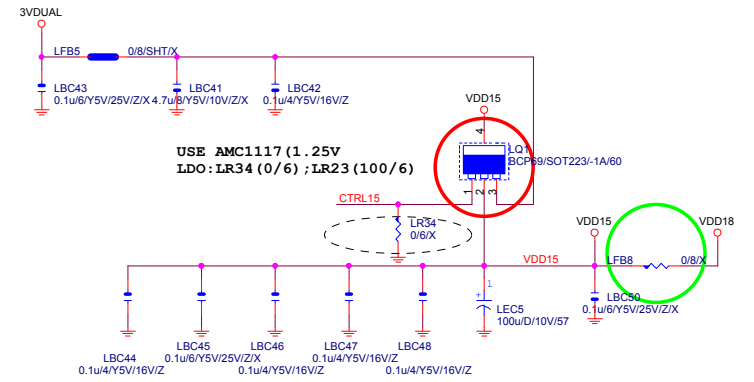
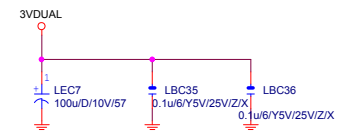
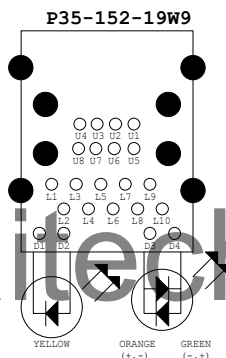
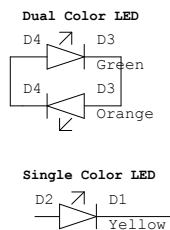
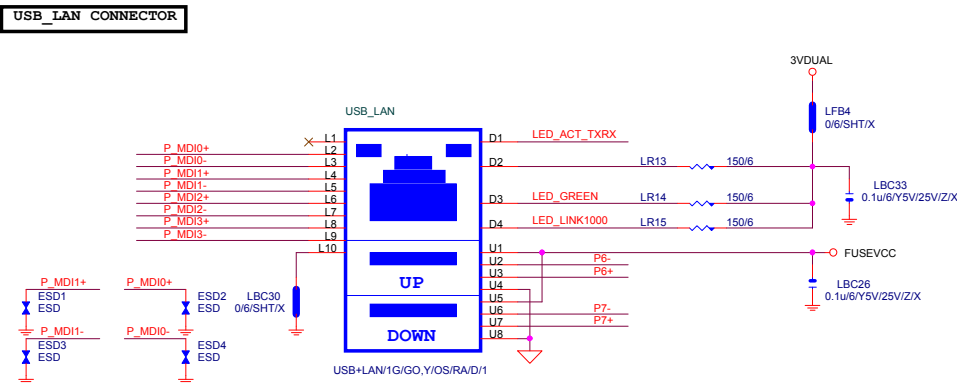
368 issue



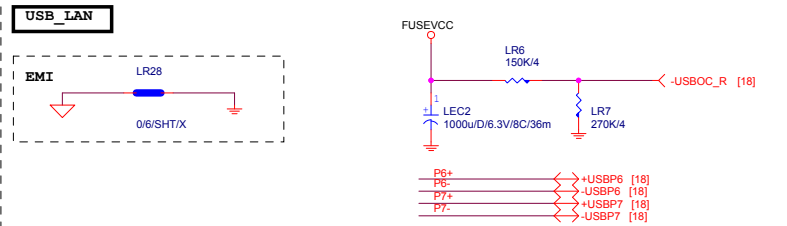
PCIE-1G LAN



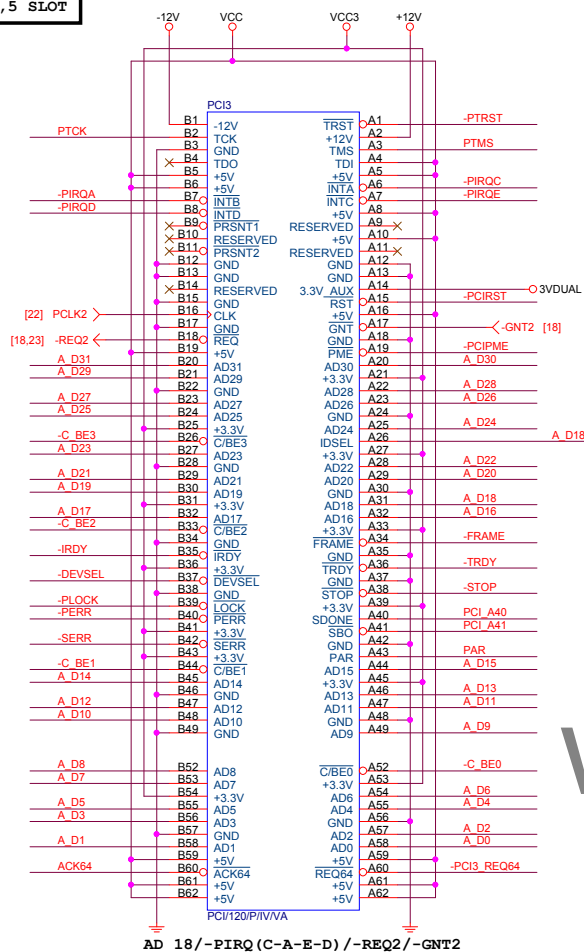
USB LAN CONNECTOR



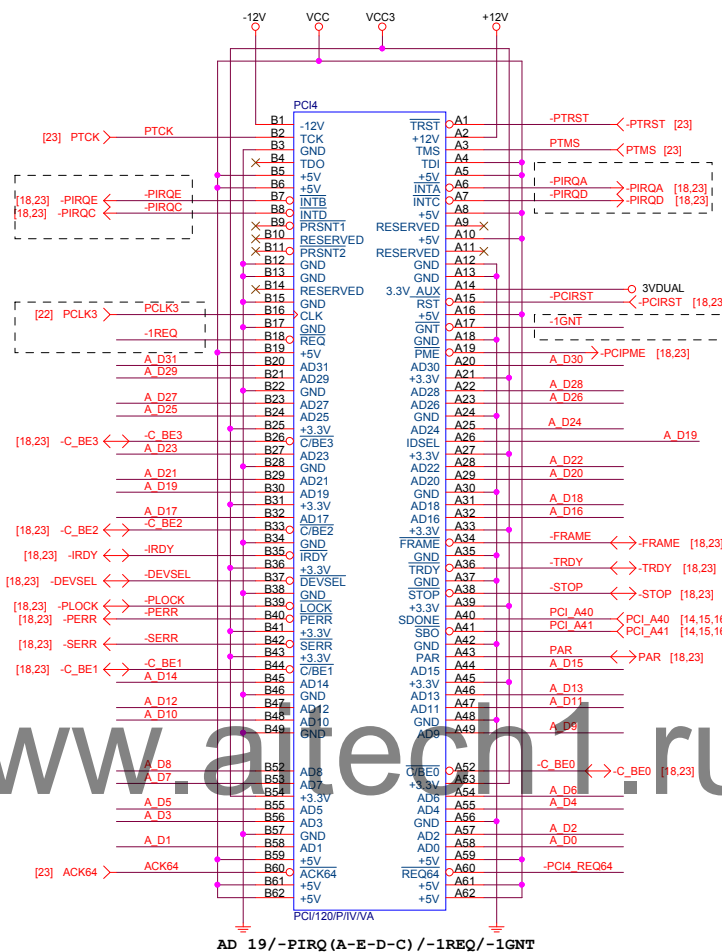
USB LAN



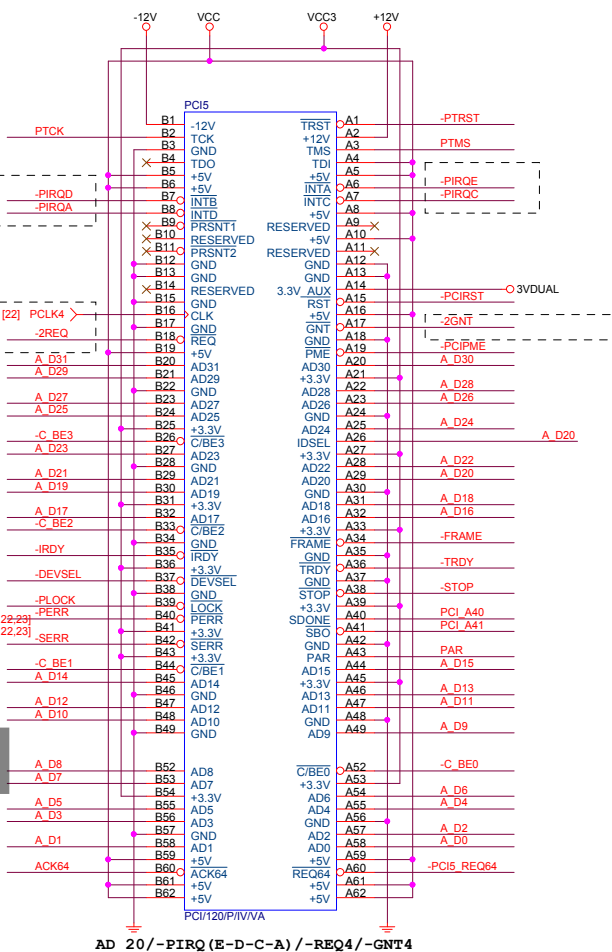
PCI 3,4,5 SLOT



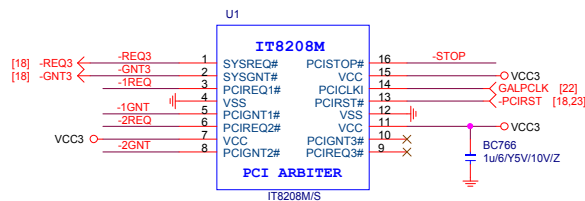
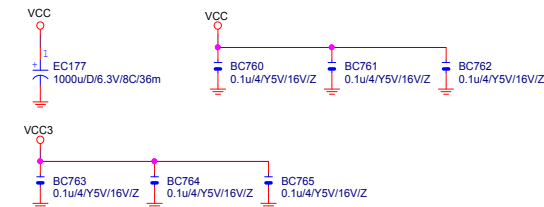
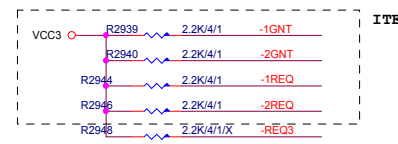
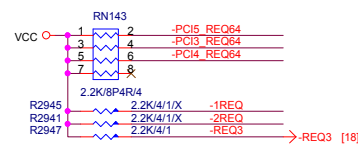
AD 18/-PIRQ(C-A-E-D) /-REQ2/-GNT2



AD 19/-PIRQ (A-E-D-C) /-1REQ/-1GNT



AD 20/-PIRQ (E-D-C-A) /-REQ4/-GNT4



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1.0

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